National Semiconductor

PRELIMINARY
November 1992

HPC36400E/HPC46400E
High-Performance Communications MicroController

General Description

The HPC46400E is an upgraded HPC16400. Features have been added to support V.120, the 8-bit mode has been enhanced to support all instructions, and the UART has been changed to provide more flexibility and power. The HPC46400E is fully upward compatible with the HPC16400.

The HPC46400E has 4 functional blocks to support a wide range of communication application-2 HDLC channels, 4 channel DMA controller to facilitate data flow for the HDLC channels, programmable serial interface and UART.

The serial interface decoder allows the 2 HDLC channels to be used with devices using interchip serial link for point-to-point and multipoint data exchanges. The decoder generates enable signals for the HDLC channels allowing multiplexed D and B channel data to be accessed.

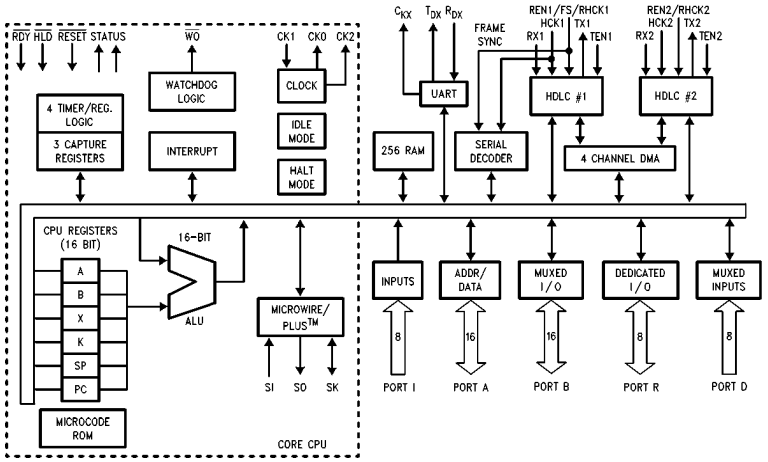
The HDLC channels manage the link by providing sequencing using the HDLC framing along with error control based upon a cyclic redundancy check (CRC). Multiple address recognition modes, and both bit and byte modes of operation are supported.

The HPC36400E and HPC46400E are available in 68-pin PLCC and 80-pin PQFP packages.

Features

- HPC™ family—core features:
  - — 16-bit data bus, ALU, and registers
  - — 64 kbytes of external memory addressing
  - — FAST!—20.0 MHz system clock
  - — Four 16-bit timer/counters with WATCHDOG™ logic
  - — MICROWIRE/PLUS™ serial I/O interface
  - — CMOS—low power with two power save modes
- Two full duplex HDLC channels
  - — Optimized for ISDN, X.25, V.120, and LAPD applications
  - — Programmable frame address recognition
  - — Up to 4.65 Mbps serial data rate
  - — Built in diagnostics
  - — Synchronous bypass mode
  - — Optional CRC generation
  - — Received CRC bytes can be read by the CPU
- Four channel DMA controller
- 8- or 16-bit external data bus
- UART
  - — Full duplex
  - — 7, 8, or 9 data bits
  - — Even, odd, mark, space or no parity
  - — 7/8, 1 or 2 stop bit generation
  - — Accurate internal baud rate generation up to 625k baud without penalty of using expensive crystal
  - — Synchronous and asynchronous modes of operation
- Serial Decoder
  - — Supports 6 popular time division multiplexing protocols for inter-chip communications
  - — Optional rate adaptation of 64 kbit/s data rate to 56 kbit/s
- Over ½ Mbyte of extended addressing
- Easy interface to National's DASL, 'U' and 'S' transceivers—TP3400, TP3410 and TP3420
- Commercial (0°C to +70°C) and industrial (−40°C to +85°C)

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	(V_{CC} + 0.5)V to (GND − 0.5)V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC_1}	Supply Current	V_{CC} = 5.5V, f_{in} = 20.0 MHz (Note 1)		70	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		10	mA
I_{CC_2}	IDLE Mode Current	V_{CC} = 5.5V, f_{in} = 20.0 MHz (Note 1)		10	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		2	mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.5V, f_{in} = 0 kHz (Note 1)		500	μA
		V_{CC} = 2.5V, f_{in} = 0 kHz (Note 1)		150	μA
INPUT VOLTAGE LEVELS—SCHMITT TRIGGERED: $\overline{RESET}$, $\overline{WO}$, D0, NMI, I2, I3; AND ALSO CKI					
V_{IH_1}	Logic High		0.9 V_{CC}		V
V_{IL_1}	Logic Low			0.1 V_{CC}	V
INPUT VOLTAGE LEVELS—PORT A					
V_{IH_2}	Logic High		2.0		V
V_{IL_2}	Logic Low			0.8	V
INPUT VOLTAGE LEVELS—ALL OTHERS					
V_{IH_3}	Logic High		0.7 V_{CC}		V
V_{IL_3}	Logic Low			0.2 V_{CC}	V
I_{LI}	Input Leakage Current	(Note 2)		±1	μA
C_I	Input Capacitance	(Note 3)		10	pF
C_{IO}	I/O Capacitance	(Note 3)		20	pF
OUTPUT VOLTAGE LEVELS					
V_{OH_1}	Logic High (CMOS)	I_{OH} = −10 μA (Note 3)	V_{CC} − 0.1		V
V_{OL_1}	Logic Low (CMOS)	I_{OL} = 10 μA (Note 3)		0.1	V
V_{OH_2}	Port A/B Drive, CK2 (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −1 mA	2.4		V
V_{OL_2}		I_{OL} = 3 mA		0.4	V
V_{OH_3}	Other Port Pin Drive, $\overline{WO}$ (open drain) (B_0–B_9, B_{13}, B_{14}, R_0–R_7, D_5, D_7)	I_{OH} = −1.6 mA (except $\overline{WO}$)	2.4		V
V_{OL_3}		I_{OL} = 0.5 mA		0.4	V
V_{OH_4}	ST1 and ST2 Drive	I_{OH} = −6 mA	2.4		V
V_{OL_4}		I_{OL} = 1.6 mA (Note 4)		0.4	V
V_{RAM}	RAM Keep-Alive Voltage	(Note 5)	2.5		V
I_{OZ}	TRI-STATE Leakage Current	V_{IN} = 0 and V_{IN} = V_{CC}		±5	μA

Note 1: I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0). I_{CC_1} is measured with $\overline{RESET}$ = V_{SS}. I_{CC_3} is measured with NMI = V_{CC}. CKI driven to V_{IH_1} and V_{IL_1} with rise and fall times less than 10 ns.

Note 2: $\overline{RDY}$/$\overline{HLD}$ and $\overline{RDY}$/I4 pins have internal pullups and meet this spec only at V_{IN} = V_{CC}.

Note 3: These parameters are guaranteed by design and are not tested.

Note 4: ST2 drive will not meet this spec under condition of RESET pin = low.

Note 5: Test duration is 100 ms.

AC Electrical Characteristics

(see Notes 1 and 4 and *Figures 1* thru *5*), V_{CC} = 5V ±10%, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E

	Symbol and Formula	Parameter and Notes	Min	Max	Units	Note
Clocks	f_C	Operating Frequency	2	20	MHz	
	$t_{C1} = 1/f_C$	Operating Period	50	500	ns	
	t_{CKIH}	CKI Rise Time	22.5		ns	
	t_{CKIL}	CKI Fall Time	22.5		ns	
	$t_C = 2/f_C$	CPU or DMA Timing Cycle	100		ns	
	$t_{WAIT} = t_C$	CPU or DMA Wait State Period	100		ns	
	t_{DC1C2R}	Delay of CK2 Rising Edge after CKI Falling Edge	0	55	ns	(Note 2)
	t_{DC1C2F}	Delay of CK2 Falling Edge after CKI Falling Edge	0	55	ns	(Note 2)
	$f_U = f_C/8$	External UART Clock Input Frequency		2.5	MHz	
	f_{MW}	External MICROWIRE/PLUS Clock Input Frequency		1.25	MHz	
	$t_{HCK} = 4t_{C1} + 14$	HDLC Clock Input Period	214		ns	
Timers	$f_{XIN} = f_C/22$	External Timer Input Frequency		0.91	kHz	
	$t_{XIN} = t_C$	Pulse Width for Timer Inputs	100		ns	
MICROWIRE/PLUS	t_{UWS}	MICROWIRE Setup Time — Master — Slave	100 20		ns ns	
	t_{UWH}	MICROWIRE Hold Time — Master — Slave	20 50		ns ns	
	t_{UWV}	MICROWIRE Output Valid Time — Master — Slave		50 150	ns ns	
External Hold	$t_{SALE} = \frac{3}{4}\,t_C + 40$	$\overline{HLD}$ Falling Edge before ALE Rising Edge	115		ns	
	$t_{HWP} = \frac{3}{4}\,t_C + 35$	$\overline{HLD}$ Pulse Width	110		ns	
	$t_{HAE} = \frac{3}{4}\,t_C + 100$	$\overline{HLDA}$ Falling Edge after $\overline{HLD}$ Falling Edge		175	ns	(Note 3)
	$t_{HAD} = \frac{5}{4}\,t_C + 85$	$\overline{HLDA}$ Rising Edge after $\overline{HLD}$ Rising Edge		210	ns	
	t_{BF}	Bus Float after $\overline{HLDA}$ Falling Edge		66	ns	
	$t_{BE} = t_C - 66$	Bus Enable after $\overline{HLDA}$ Rising Edge	34		ns	

Note 1: These AC characteristics are guaranteed with external clock drive on CKI having 50% duty cycle and with less than 15 pF load on CKO. Spec'd t_{C1R}, t_{C1F}, and CKI duty cycle limits are not tested but are guaranteed functional by design. Keep in mind that when SLOW mode is selected, f_C (Operating Frequency) will be the external frequency divided by 4 and that value should be used in all formulas relating to the AC Characteristics.

Note 2: Do not design with this parameter unless CKI is driven with an active signal and SLOW mode is not selected. When using a passive crystal circuit, its stability is not guaranteed if either CKI or CKO is connected to any external logic other than the passive components of the crystal circuit.

Note 3: t_{HAE} is spec'd for case with $\overline{HLD}$ falling edge occurring at the latest time it can be accepted during the present CPU or DMA cycle being executed. If $\overline{HLD}$ falling edge occurs later, t_{HAE} as long as (3 t_C + 4 WS + 72 t_C + 100) may occur depending on the following CPU instruction or DMA cycle, its wait states and ready input.

Note 4: WS (t_{WAIT}) × (number of preprogrammed wait states). Minimum and maximum values are calculated at maximum operating frequency, f_C = 20 MHz, with one wait state preprogrammed. These values are guaranteed with AC loading of 100 pF on Port A, 50 pF on CK2, 80 pF on other outputs, and DC loading of the pin's DC spec non CMOS I_{OL} or I_{OH}.

AC Electrical Characteristics (Continued)

CPU and DMA Timing (see Notes 1 and 4 and *Figures 2, 4, 6, 7, 8,* and *9*), V_{CC} = 5V ±10%, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E

	Symbol	Formula	Cycle	Parameter	Min	Max	Units	Note
Address Cycles	t_{1ALR}		CPU DMA	Delay of ALE Rising Edge after CKI Rising Edge Delay of ALE Rising Edge after CKI Falling Edge	0 0	35 35	ns ns	(Note 2) (Note 2)
	t_{1ALF}		CPU DMA	Delay of ALE Falling Edge after CKI Rising Edge Delay of ALE Falling Edge after CKI Falling Edge	0 0	35 35	ns ns	(Note 2) (Note 2)
	t_{2ALR}	$\frac{1}{4} t_C + 20$	CPU	ALE Rising Edge after CK2 Rising Edge		45	ns	
	t_{2ALF}	$\frac{1}{4} t_C + 20$	CPU	ALE Falling Edge after CK2 Falling Edge		45	ns	
	t_{LL}	$\frac{1}{2} t_C - 9$		ALE Pulse Width	41		ns	
	t_{ST}	$\frac{1}{4} t_C - 20$		Setup of Address Valid before ALE Falling Edge	5		ns	(Note 3)
	t_{VP}	$\frac{1}{4} t_C - 10$ $\frac{1}{2} t_C - 10$	CPU DMA	Hold of Address Valid after ALE Falling Edge	15 40		ns ns	
Read Cycles	t_{ARR}	$\frac{1}{2} t_C - 20$		ALE Falling Edge to $\overline{RD}$ Falling Edge	30		ns	
	t_{ACC}	$t_C + WS - 55$ $\frac{5}{4} t_C + WS - 75$	CPU DMA	Data Input Valid after Address Output Valid		145 150	ns ns	
	t_{RD}	$\frac{1}{4} t_C + WS - 35$ $\frac{1}{2} t_C + WS$	CPU DMA	Data Input Valid after $\overline{RD}$ Falling Edge		90 115	ns ns	
	t_{RW}	$\frac{1}{4} t_C + WS - 15$ $\frac{1}{2} t_C + WS - 15$	CPU DMA	$\overline{RD}$ Pulse Width	110 135		ns ns	
	t_{DR}	$\frac{3}{4} t_C - 25$		Hold of Data Input Valid after $\overline{RD}$ Rising Edge	0	50	ns	
	t_{RDA}	$\frac{3}{4} t_C - 20$		Bus Enable after $\overline{RD}$ Rising Edge	55		ns	
Write Cycles	t_{ARW}	$\frac{1}{2} t_C - 20$		ALE Falling Edge to $\overline{WR}$ Falling Edge	30		ns	
	t_{WW}	$\frac{3}{4} t_C + WS - 15$ $\frac{1}{2} t_C + WS - 15$	CPU DMA	$\overline{WR}$ Pulse Width	160 135		ns ns	
	t_V	$\frac{1}{2} t_C + WS - 40$ $\frac{1}{2} t_C + WS - 50$	CPU DMA	Data Output Valid before $\overline{WR}$ Rising Edge	110 100		ns ns	
	t_{HW}	$\frac{1}{4} t_C - 10$		Hold of Data Output Valid after $\overline{WR}$ Rising Edge	15		ns	(Note 5)
Ready Input	t_{RDYS}			$\overline{RDY}$ Falling Edge before CK2 Rising Edge	45		ns	
	t_{RDYH}			$\overline{RDY}$ Rising Edge after CK2 Rising Edge	0		ns	
	t_{RDYV}	$WS - \frac{1}{4} t_C - 47$ $t_C - 47$	CPU DMA	$\overline{RDY}$ Falling Edge after $\overline{RD}$ or $\overline{WR}$ Falling Edge		28 53	ns ns	(Note 6)

Note 1: These AC characteristics are guaranteed with external clock drive on CKI having 50% duty cycle and with less than 15 pF load on CKO. Spec'd t_{C1R}, t_{C1F}, and CKI duty cycle limits are not tested but are guaranteed functional by design. Keep in mind that when SLOW mode is selected, f_C (Operating Frequency) will be the external frequency divided by 4 and that value should be used in all formulas relating to the AC Characteristics.

Note 2: Do not design with this parameter unless CKI is driven with an active signal meeting T_{C1R} and T_{C1F} specs. When using a passive crystal circuit, its stability is not guaranteed if either CKI or CKO is connected to any external logic other than the passive components of the crystal circuit.

Note 3: Setup of HBE valid before ALE falling edge is 0 ns minimum. Setup of BS0 thru BS3 valid before ALE falling edge when in extended addressing mode is 0 ns minimum.

Note 4: WS (t_{WAIT}) × (number of preprogrammed wait states). Minimum and maximum values are calculated at maximum operating frequency, f_C = 20 MHz, with one wait state preprogrammed. These values are guaranteed with AC loading of 100 pF on Port A, 50 pF on CK2, 80 pF on other outputs, and DC loading of the pin's DC spec non CMOS I_{OL} or I_{OH}.

Note 5: Hold of HBE Output Valid after $\overline{WR}$ rising edge is 0 ns minimum. Hold of BS0 thru BS3 Output Valid after $\overline{WR}$ rising edge when in extended addressing mode is 0 ns minimum.

Note 6: In HPC in-circuit emulators the t_{RDYV} formulas are WS − ¼ t_C − 57 and t_C − 57 yielding minimums of 18 ns and 43 ns for CPU and DMA cycles, respectively.

Timing Waveforms

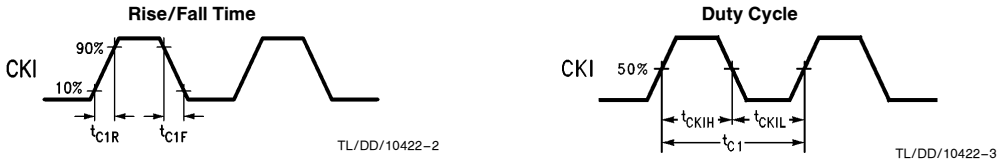

FIGURE 1. CKI Input Signal

Note: AC testing inputs are driven at V_{IH} for a logic "1" and V_{IL} for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and at 0.8V for a logic "0".

FIGURE 2. Input and Output for AC Tests

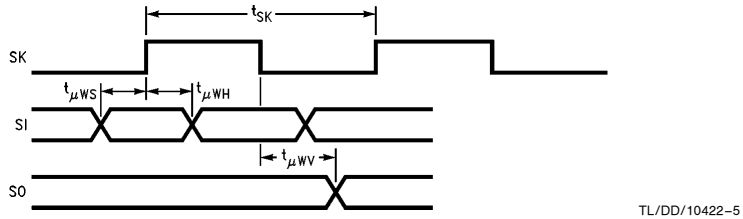

FIGURE 3. MICROWIRE Setup/Hold Timing

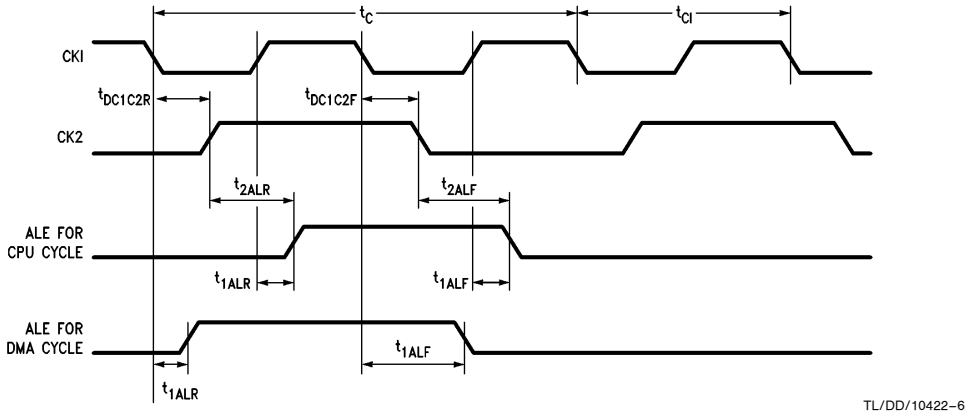

FIGURE 4. CKI, CK2 ALE Timing Diagram

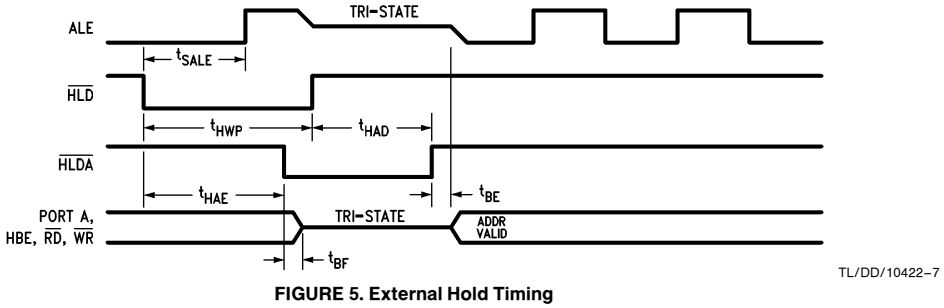

FIGURE 5. External Hold Timing

Timing Waveforms (Continued)

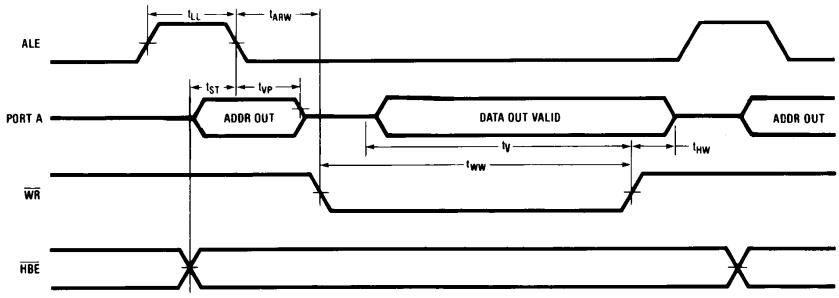

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FIGURE 6. CPU and DMA Write Cycles

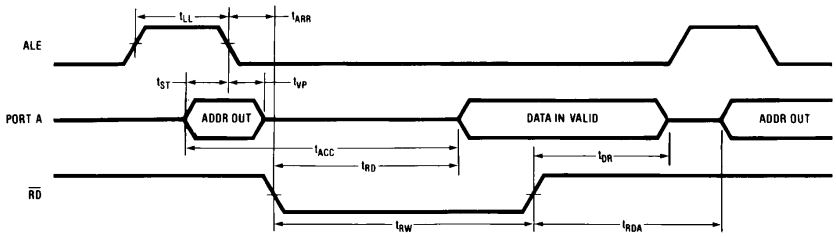

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FIGURE 7. CPU and DMA Read Cycles

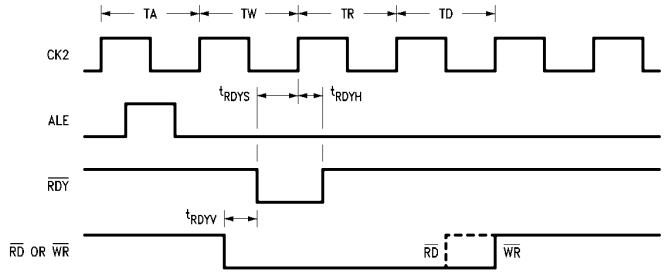

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FIGURE 8. CPU Ready Mode with 1 Wait State and Ready Wait Extension

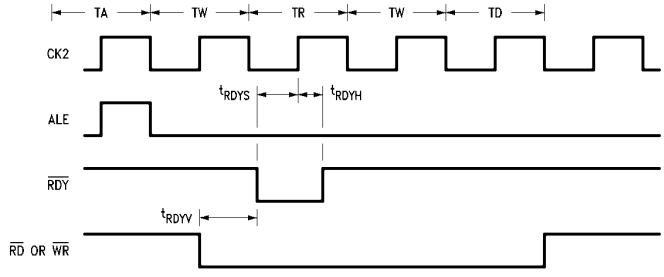

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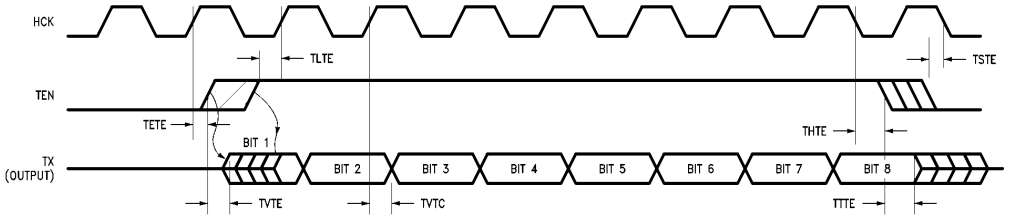
FIGURE 9. DMA Ready Mode with 2 Wait States and Ready Wait Extension

Timing Waveforms (Continued)

Timing Diagrams for TX Using External Enable



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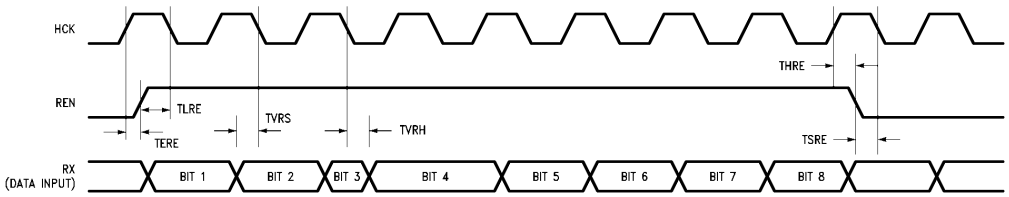
Symbol	Parameter	Min	Max	Units
TETE	Hold of TEN Low after HCK Rising Edge	5		ns
TLTE	Setup of TEN Rising Edge before HCK Rising Edge	85		ns
TVTE	Delay of TX Output Valid after TEN Rising Edge		40	ns
TVTC	Delay of TX Output Valid after HCK Rising Edge		65	ns
THTE	Hold of TEN High after HCK Falling Edge	60		ns
TSTE	Setup of TEN Falling Edge before HCK Falling Edge	20		ns
TTTE	Delay of TX Output TRI-STATE® after TEN Falling Edge		40	ns
TVTR	TVTC in Rate Adaptation Mode		75	ns

Timing Diagrams for RX Using External Enable



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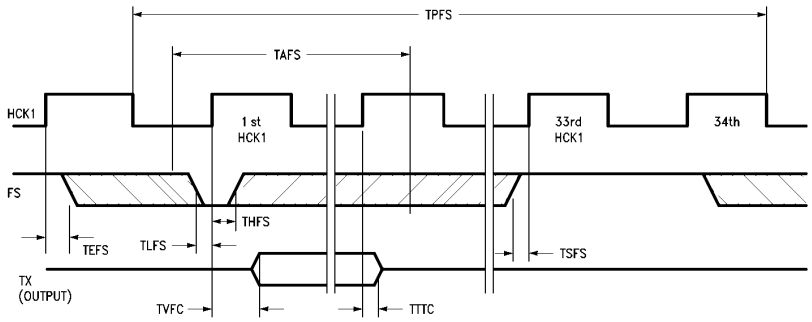
Symbol	Parameter	Min	Max	Units
TERE	Hold of REN Low after HCK Rising Edge	5		ns
TLRE	Setup of REN Rising Edge before HCK Falling Edge	30		ns
TVRS	Setup of RX Data Input Valid before HCK Falling Edge	20		ns
TVRH	Hold of RX Data Input Valid after HCK Falling Edge	20		ns
THRE	Hold of REN High after HCK Rising Edge	5		ns
TSRE	Setup of REN Falling Edge before HCK Falling Edge	30		ns

Timing Waveforms (Continued)

Serial Decoder Timing Diagram (Mode 2)



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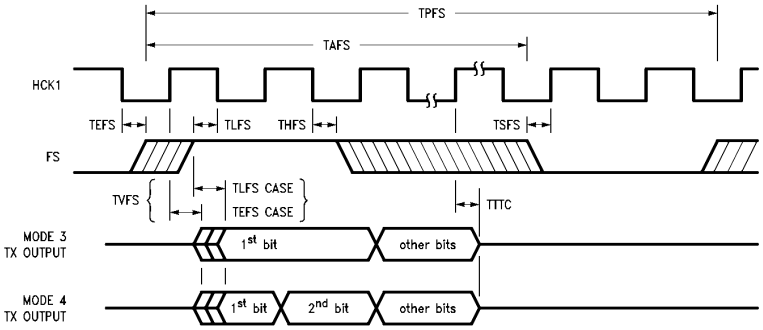
Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Falling Edges	34			
TAFS	Number of HCK1 Rising Edges during FS Low	1	32		
TEFS	Hold of FS High after HCK1 Rising Edge	10		Early FS	ns
TLFS	Setup of FS Falling Edge before HCK1 Rising Edge	20		Late FS, (Note 8)	ns
TVFC	Delay of TX Output Valid after HCK1 Rising Edge		60	(Note 7)	ns
THFS	Hold of FS Low after HCK1 Rising Edge	20			ns
TSFS	Setup of FS Rising Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns
TVFR	TVFC in Rate Adaptation Mode		75		ns

Serial Decoder Timing Diagram (Modes 3, 4)



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Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Rising Edges	64		SD Mode 3	
TPFS	Number of HCK1 Periods between FS Rising Edges	32		SD Mode 4	
TAFS	Number of HCK1 Falling Edges during FS High	2	62	SD Mode 3	
TAFS	Number of HCK1 Falling Edges during FS High	2	30	SD Mode 4	
TEFS	Hold of FS Low after HCK1 Falling Edge	10		Early FS	ns
TLFS	Setup of FS Rising Edge before HCK1 Falling Edge	45		Late FS, (Note 8)	ns
TVFS	Delay of TX Output Valid after HCK1 and FS Rising Edges		70	(Note 9)	ns
THFS	Hold of FS High after HCK1 Falling Edge	20			ns
TSFS	Setup of FS Falling Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns

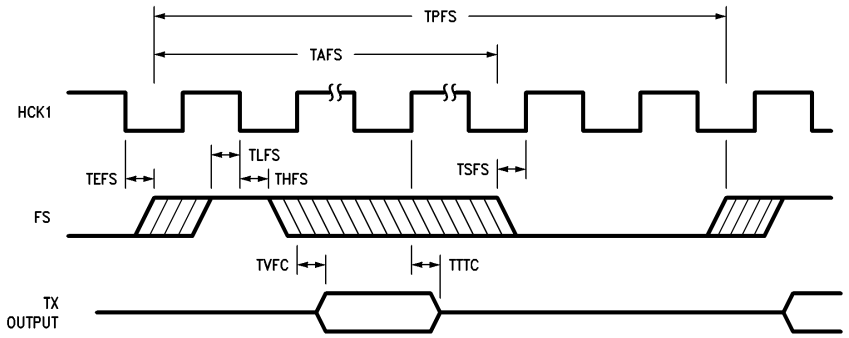
Note 7: This spec is for 1st bit only. Remaining bits are spec'd by transmitter TVTC spec.

Note 8: Receiver specs TVRS and TVRH are required along with TLFS for receiver operation using serial decoder.

Note 9: This spec is for 1st bit only and is measured from the later of either FS or HCK1 rising edge. Remaining bits are spec'd from HCK1 rising edges by transmitter TVTC spec.

Timing Waveforms (Continued)

Serial Decoder Timing Diagram (Modes 5, 6,7)



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Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Rising Edges	34			
TAFS	Number of HCK1 Falling Edges during FS High	1	32		
TEFS	Hold of FS Low after HCK1 Falling Edge	10		Early FS	ns
TLFS	Setup of FS Rising Edge before HCK1 Falling Edge	45		Late FS, (Note 8)	ns
TVFC	Delay of TX Output Valid after HCK1 Rising Edge		60	(Note 7)	ns
THFS	Hold of FS High after HCK1 Falling Edge	20			ns
TSFS	Setup of FS Falling Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns

Note 7: This spec is for 1st bit only. Remaining bits are spec'd by transmitter TVTC spec.

Note 8: Receiver specs TVRS and TVRH are required along with TLFS for receiver operation using serial decoder.

Pin Descriptions

I/O PORTS

Port A is a 16-bit multiplexed address/data bus used for accessing external program and data memory. Four associated bus control signals are available on port B. The Address Latch Enable (ALE) signal is used to provide timing to demultiplex the bus. Reading from and writing to external memory are signalled by $\overline{RD}$ and $\overline{WR}$ respectively. External memory can be addressed as either bytes or words with the decoding controlled by two lines, Bus High Byte enable ($\overline{HBE}$) and Address/Data Line 0 (A0).

Port B is a 16-bit port, with 12 bits of bidirectional I/O. Pins B10, B11, B12 and B15 are the control bus signals for the address/data bus. Port B may also be configured via a function register BFUN to individually allow each bidirectional I/O pin to have an alternate function.

B0:	TDX	UART Data Output
B1:	CFLG1	Closing Flag Output for HDLC #1 Transmitter
B2:	CKX	UART Clock (Input or Output)
B3:	T2IO	Timer2 I/O Pin
B4:	T3IO	Timer3 I/O Pin
B5:	SO	MICROWIRE/PLUS Output
B6:	SK	MICROWIRE/PLUS Clock (Input or Output)
B7:	$\overline{HLDA}$	Hold Acknowledge Output
B8:	TS0	Timer Synchronous Output
B9:	TS1	Timer Synchronous Output
B10:	ALE	Address Latch Enable Output for Address/Data Bus
B11:	$\overline{WR}$	Address/Data Bus Write Output
B12:	$\overline{HBE}$	High Byte Enable Output for Address/Data Bus; also 8-Bit Mode Strap Input on Reset.
B13:	TS2	Timer Synchronous Output
B14:	TS3	Timer Synchronous Output
B15:	$\overline{RD}$	Address/Data Bus Read Output

When operating in the extended memory addressing mode, four bits of port B can be used as follows—

B8:	BS0	Memory bank switch output 0 (LSB)
B9:	BS1	Memory bank switch output 1
B13:	BS2	Memory bank switch output 2
B14:	BS3	Memory bank switch output 3 (MSB)

Port I is an 8-bit input port that can be read as general purpose inputs and can also be used for the following functions:

I0:	HCK2	HLDC #2 Clock Input
I1:	NMI	Nonmaskable Interrupt Input
I2:	INT2	Maskable Interrupt/Input Capture
I3:	INT3	Maskable Interrupt/Input Capture
I4:	INT4/RDY	Maskable Interrupt/Input Capture/ Ready Input
I5:	SI	MICROWIRE/PLUS Data Input
I6:	RDX	UART Data Input
I7:	HCK1	HDLC #1 Clock and Serial Decoder Clock Input

Port D is an 8-bit input port that can be read as general purpose inputs and can also be used for the following functions:

D0:	REN1/FS/ RHCK1	Receiver #1 Enable/Serial Decoder Frame Sync Input/Receiver #1 Clock Input
D1:	TEN1	Transmitter #1 Enable Input
D2:	REN2/ RHCK2	Receiver #2 Enable Input/Receiver #2 Clock Input
D3:	TEN2	Transmitter #2 Enable Input
D4:	RX1	Receiver #1 Data Input
D5:	TX1	Transmitter #1 Data Output
D6:	RX2	Receiver #2 Data Input
D7:	TX2	Transmitter #2 Data Output

Note: Any of these pins can be read by software. Therefore, unused functions can be used as general purpose inputs, notably external enable lines when the internal serial decoder is used.

Port R is an 8-bit bidirectional I/O port available for general purpose I/O operations. Port R has a direction register to enable each separate pin to be individually defined as an input or output. It has a data register which contains the value to be output. In addition, the Port R pins can be read directly using the Port R pins address.

Pin Descriptions (Continued)

POWER SUPPLIES

V_{CC1}, V_{CC2}	Positive Power Supply (two pins)
GND	Ground for On-Chip Logic
DGND	Ground for Output Buffers

Note: There are multiple electrically connected V_{CC} pins on the chip, GND and DGND are electrically isolated. All V_{CC} pins and all ground pins must be used.

CLOCK PINS

CKI	The System Clock Input
CKO	The System Clock Output (Inversion of CKI)

Pins CKI and CKO are usually connected across an external crystal.

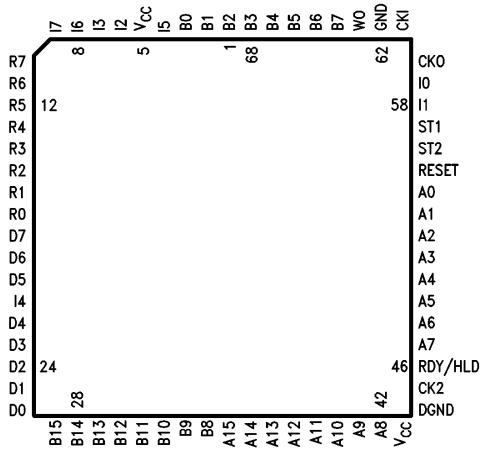
CK2	Clock Output (CKI divided by 2)

OTHER PINS

$\overline{WO}$	This is an active low open drain output which signals an illegal situation has been detected by the WATCHDOG logic.
ST1	Bus Cycle Status Output indicates first op-code fetch.
ST2	Bus Cycle Status Output indicates machine states (skip and interrupt).
$\overline{RESET}$	Active low input that forces the chip to restart and sets the ports in a TRI-STATE mode.
RDY/$\overline{HLD}$	Has two uses, selected by a software bit. This pin is either a READY input to extend the bus cycle for slower memories or a HOLD-REQUEST input to put the bus in a high impedance state for external DMA purposes. In the second case the I4 pin can become the READY input.

Connection Diagrams

Plastic and Leaded Chip Carriers



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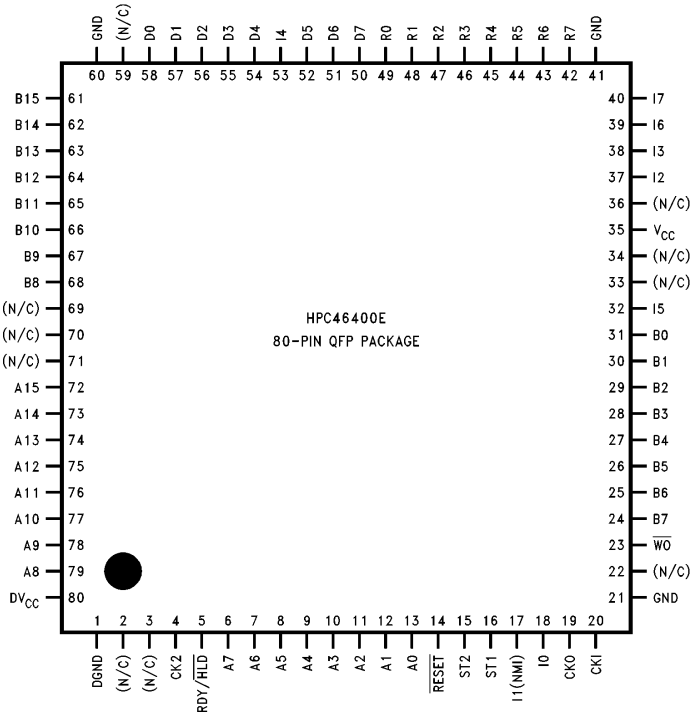
Top View

See NS Package Number V68A

Connection Diagrams (Continued)



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Top View

See NS Package Number VHG80A

Wait States

The HPC46400E provides software selectable Wait States for access to slower memories and for shared bus applications. The number of Wait States for the CPU are selected by two bits in the PSW register. The number of Wait States for DMA are selected by a bit in the Message System Configuration register. Additionally, the RDY input may be used to extend the RD or WR cycle, allowing the HPC to be used in shared memory applications and allowing the user to interface with slow memories and peripherals.

Power Save Modes

Two power saving modes are available on the HPC46400E: HALT and IDLE. In the HALT mode, all processor activities are stopped. In the IDLE mode, the on-board oscillator and timer T0 are active but all other processor activities are stopped. In either mode, on-board RAM, registers and I/O are unaffected (except the HDLC and UART which are reset).

HALT MODE

The HPC46400E is placed in the HALT mode under software control by setting bits in the PSW. All processor activities, including the clock and timers, are stopped. In the HALT mode, power requirements for the HPC46400E are minimal and the applied voltage (V_{CC}) may be decreased without altering the state of the machine. There are two ways of exiting the HALT mode: via the $\overline{\text{RESET}}$ or the NMI. The $\overline{\text{RESET}}$ input reinitializes the processor. Use of the NMI input will generate a vectored interrupt and resume operation from that point with no initialization. The HALT mode can be enabled or disabled by means of a control register HALT enable. To prevent accidental use of the HALT mode the HALT enable register can be modified only once.

IDLE MODE

The HPC46400E is placed in the IDLE mode through the PSW. In this mode, all processor activity, except the on-board oscillator and Timer T0, is stopped. The HPC46400E resumes normal operation upon timer T0 overflow. As with the HALT mode, the processor is also returned to full operation by the $\overline{\text{RESET}}$ or NMI inputs, but without waiting for oscillator stabilization.

SLOW MODE

The HPC46400E is placed in the SLOW mode under software control by setting ''SLOW'' bit in ''FEXT'' Feature Extension register. In this mode CKI is divided by 4 and each CK2 cycle will be 8 CKI clock cycles. This reduction in frequency of operation of HPC16400E is achieved without altering the state of the machine. CKI and CKO signals remain unaffected reagardless of the status of the SLOW bit. At $\overline{\text{RESET}}$ the ''SLOW'' bit comes up as 0, i.e., the clocking of the HPC46400E is normal. Software can cause the division to be enabled or disabled by writing a 1 or a 0 to the ''SLOW'' bit. Note that when the ''SLOW'' bit is set to 1, HALT or IDLE power down mode cannot be entered, ''SLOW'' bit has to be cleared to a 0 first.

HPC46400E Interrupts

Complex interrupt handling is easily accomplished by the HPC46400E's vectored interrupt scheme. There are eight possible interrupt sources as shown in Table I.

TABLE I. Interrupts

Vector/ Address	Interrupt Source	Arbitration Ranking
FFFF|FFFE	Reset	0
FFFD|FFFC	Nonmaskable Ext (NMI)	1
FFFB|FFFA	External on I2	2
FFF9|FFF8	External on I3	3
FFF7|FFF6	External on I4	4
FFF5|FFF4	Internal on Timers	5
FFF3|FFF2	Internal on UART	6
FFF1|FFF0	End of Message (EOM)	7

The HPC46400E contains arbitration logic to determine which interrupt will be serviced first if two or more interrupts occur simultaneously. Interrupts are serviced after the current instruction is completed except for the RESET which is serviced immediately.

The NMI interrupt will immediately stop DMA activity. Byte transfers in progress will finish thereby allowing an orderly transition to the interrupt service vector (see DMA description). The HDLC channels continue to operate, and the user must service data errors that might have occurred during the NMI service routine.

Interrupt Processing

Interrupts are serviced after the current instruction is completed except for the RESET, which is serviced immediately.

RESET holds on-chip logic in a reset state while low, and triggers the RESET interrupt on its rising edge. All other interrupts are edge-sensitive. NMI is positive-edge sensitive. The external interrupts on I2, I3, and I4 can be software selected to be rising or falling edge sensitive.

Interrupt Control Registers

The HPC46400E allows the various interrupt sources and conditions to be programmed. This is done through the various control registers. A brief description of the different control registers is given below.

INTERRUPT ENABLE REGISTER (ENIR)

RESET and the External Interrupt on I1 are non-maskable interrupts. The other interrupts can be individually enabled or disabled. Additionally, a Global Interrupt Enable Bit in the ENIR Register allows the Maskable interrupts to be collectively enabled or disabled. Thus, in order for a particular interrupt to request service, both the individual enable bit and the Global Interrupt bit (GIE) have to be set.

INTERRUPT PENDING REGISTER (IRPD)

The IRPD register contains a bit allocated for each interrupt vector. The occurrence of specified interrupt trigger conditions causes the appropriate bit to be set. There is no indication of the order in which the interrupts have been received. The bits are set independently of the fact that the interrupts may be disabled. IRPD is a Read/Write register. The bits corresponding to the external interrupts are normally cleared by the HPC46400E upon entering the interrupt servicing routine.

For the interrupts from the on-board peripherals, the user has the responsibility of acknowledging the interrupt through software.

INTERRUPT CONDITION REGISTER (IRCD)

Three bits of the register select the input polarity of the external interrupt on I2, I3, and I4.

Servicing the Interrupts

The Interrupt, once acknowledged, pushes the program counter (PC) onto the stack thus incrementing the stack pointer (SP) twice. The Global Interrupt Enable (GIE) bit is reset, thus disabling further interrupts. The program counter is loaded with the contents of the memory at the vector address and the processor resumes operation at this point. At the end of the interrupt service routine, the user does a RETI instruction to pop the stack, set the GIE bit and return to the main program. The GIE bit can be set in the interrupt service routine to nest interrupts if desired. *Figure 10* shows the Interrupt Enable Logic.

Reset

The RESET input initializes the processor and sets all pins at TRI-STATE except CK0, CK2, and WO. HBE and ST2 have pull-downs designed to withstand override. RESET is an active-low Schmitt trigger input. The processor vectors to FFFF:FFFE and resumes operation at the address contained at that memory location.

The $\overline{\text{RESET}}$ pin must be asserted low for at least 16 cycles of the CK2 clock. In applications using the WATCHDOG feature, $\overline{\text{RESET}}$ should be asserted for at least 64 cycles of the CK2 clock.

On application of power, $\overline{\text{RESET}}$ must be held low for at least five times the power supply rise time to ensure that the on-chip oscillator circuit has time to stabilize.

Timer Overview

The HPC46400E contains a powerful set of flexible timers enabling the HPC46400E to perform extensive timer functions; not usually associated with microcontrollers.

The HPC46400E contains four 16-bit timers. Three of the timers have an associated 16-bit register. Timer T0 is a free-running timer, counting up at a fixed CKI/16 (Clock Input/16) rate. It is used for WATCHDOG logic, high speed event capture, and to exit from the IDLE mode. Consequently, it cannot be stopped or written to under software control. Timer T0 permits precise measurements by means of the capture registers I2CR, I3CR, and I4CR. A control bit in the register T0CON configures timer T1 and its associated register R1 as capture registers I3CR and I2CR. The capture registers I2CR, I3CR, and I4CR respectively, record the value of timer T0 when specific events occur on the interrupt pins I2, I3, and I4. The control register IRCD programs the capture registers to trigger on either a rising edge or a falling edge of its respective input. The specified edge can also be programmed to generate an interrupt (see *Figure 11*).

The timers T2 and T3 have selectable clock rates. The clock input to these two timers may be selected from the following two sources: an external pin, or derived internally by dividing the clock input. Timer T2 has additional capability of being clocked by the timer T3 underflow. This allows the user to cascade timers T3 and T2 into a 32-bit timer/counter. The control register DIVBY programs the clock input to timers T2 and T3 (see *Figure 12*).

Timer Overview (Continued)

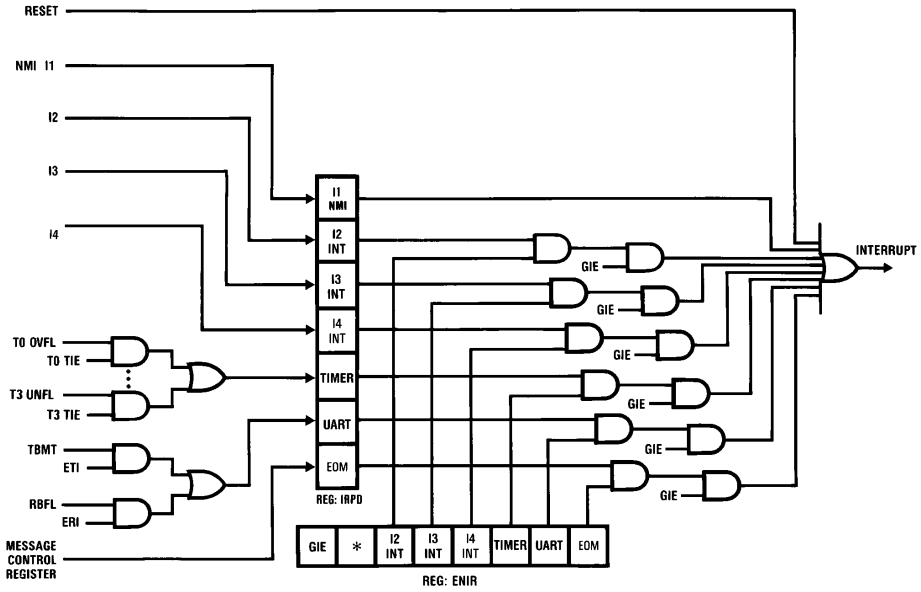

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FIGURE 10. Interrupt Enable Logic

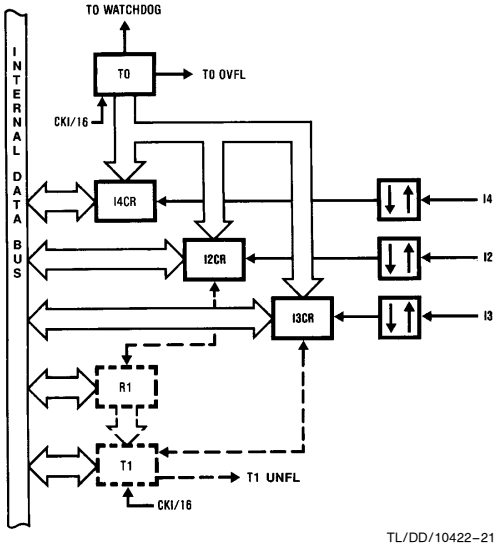

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FIGURE 11. Timers T0–T1 Block

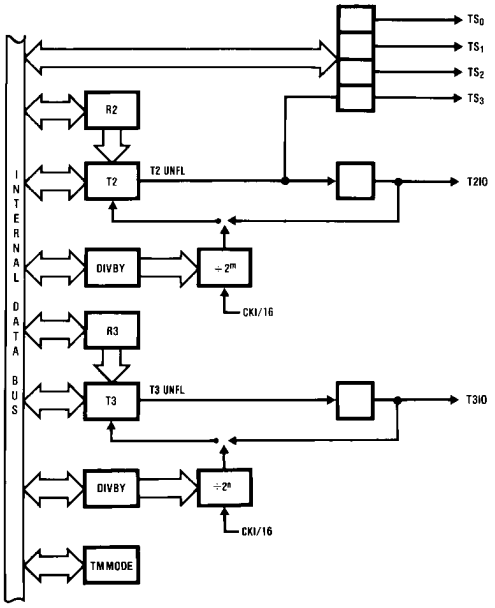

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FIGURE 12. Timers T2–T3 Block

Timer Overview (Continued)

The timers T1 through T3 in conjunction with their registers form Timer-Register pairs. The registers hold the pulse duration values. All the Timer-Register pairs can be read from or written to. Each timer can be started or stopped under software control. Once enabled, the timers count down, and upon underflow, the contents of its associated register are automatically loaded into the timer.

SYNCHRONOUS OUTPUTS

The flexible timer structure of the HPC46400E simplifies pulse generation and measurement. There are four synchronous timer outputs (TS0 through TS3) that work in conjunction with the timer T2. The synchronous timer outputs can be used either as regular outputs or individually programmed to toggle on timer T2 underflows (see *Figure 12*). Maximum output frequency for any timer output can be obtained by setting timer/register pair to zero. This then will produce an output frequency equal to ½ the frequency of the source used for clocking the timer.

Timer Registers

There are four control registers that program the timers. The divide by (DIVBY) register programs the clock input to timers T2 and T3. The timer mode register (TMMODE) contains control bits to start and stop timers T1 through T3. It also contains bits to latch, acknowledge and enable interrupts from timers T0 through T3.

Timer Applications

The use of Pulse Width Timers for the generation of various waveforms is easily accomplished by the HPC46400E.

Frequencies can be generated by using the timer/register pairs. A square wave is generated when the register value is a constant. The duty cycle can be controlled simply by changing the register value.

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FIGURE 13. Square Wave Frequency Generation

Synchronous outputs based on Timer T2 can be generated on the 4 outputs TS0–TS3. Each output can be individually programmed to toggle on T2 underflow. Register R2 contains the time delay between events. *Figure 14* is an example of synchronous pulse train generation.

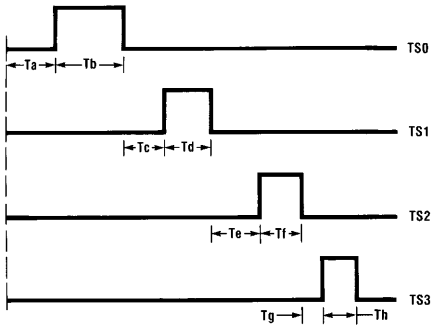

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FIGURE 14. Synchronous Pulse Generation

WATCHDOG Logic

The WATCHDOG Logic monitors the operations taking place and signals upon the occurrence of any illegal activity. The illegal conditions that trigger the WATCHDOG logic are potentially infinite loops. Should the WATCHDOG register not be written to before Timer T0 overflows twice, or more often than once every 4096 counts, an infinite loop condition is assumed to have occurred. The illegal condition forces the Watch Out (WO) pin low. The WO pin is an open drain output and can be connected to the RESET or NMI inputs or to the users external logic.

MICROWIRE/PLUS

MICROWIRE/PLUS is used for synchronous serial data communications (see *Figure 15*). MICROWIRE/PLUS has an 8-bit parallel-loaded, serial shift register using SI as the input and SO as the output. SK is the clock for the serial shift register (SIO). The SK clock signal can be provided by an internal or external source. The internal clock rate is programmable by the DIVBY register. A DONE flag indicates when the data shift is completed.

The MICROWIRE/PLUS capability enables it to interface with any of National Semiconductor's MICROWIRE peripherals (i.e., ISDN Transceivers, A/D converters, display drivers, EEPROMs).

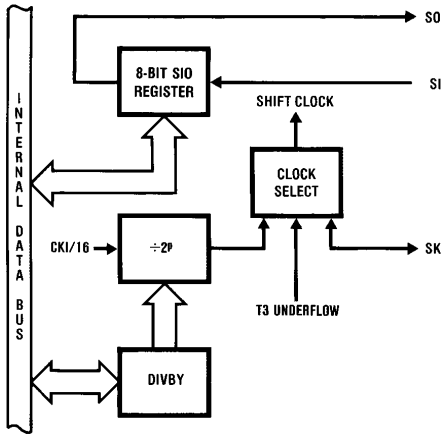

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FIGURE 15. MICROWIRE/PLUS

MICROWIRE/PLUS Operation

The HPC46400E can enter the MICROWIRE/PLUS mode as the master or a slave. A control bit in the IRCD register determines whether the HPC46400E is the master or slave. The shift clock is generated when the HPC46400E is configured as a master. An externally generated shift clock on the SK pin is used when the HPC46400E is configured as a slave. When the HPC46400E is a master, the DIVBY register programs the frequency of the SK clock. The DIVBY register allows the SK clock frequency to be programmed in 14 selectable steps from 122 Hz to 1 MHz with CKI at 16 MHz.

The contents of the SIO register may be accessed through any of the memory access instructions. Data waiting to be transmitted in the SIO register is shifted out on the falling edge of the SK clock. Serial data on the SI pin is latched in on the rising edge of the SK clock.

HPC46400E UART

The HPC46400E contains a software programmable UART. The UART (see *Figure 16*) consists of a transmit shift register, a receiver shift register and five addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR) and a UART interrupt and clock source register (ENUI). The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (7, 8 or 9 bits) and the value of the ninth bit in transmission. The ENUR register flags framing, parity, and data overrun errors while the UART is receiving. Other functions of the ENUR register include saving the ninth bit received in the data frame, reporting receiving and transmitting status, and enabling or disabling the UART's Wake-up Mode of operation. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits (7/8, 1, 1 7/8, 2), selecting between the synchronous or asynchronous mode and enabling or disabling transmit and receive interrupts.

The clock inputs to the Transmitter and Receiver sections of the UART can be individually selected to come from either an off-chip source on the CKX pin or one of the three on-chip sources. Presently, two of the on-chip sources, the Divide-By (DIVBY) Register and the Precision UART Timer (PUT), are primarily for reasons of upward compatibility from earlier HPC family members. The most flexible and accurate on-chip clocking is provided by the third source: the Baud Rate Generator (BRG).

The Baud Rate Generator is controlled by the register pair PSR and BAUD, shown below.

The Prescaler factor is selected by the upper 5 bits of the PSR register (the PRESCALE field), in units of the CK2 clock from 1 to 16 in 1/2 step increments. The lower 3 bits of the PSR register, in conjunction with the 8 bits of the baud register, form the 11-bit BAUDRATE field, which defines a baud rate divisor ranging from 1 to 2048, in units of the prescaled clock selected by the PRESCALE field.

In Asynchronous Mode, the resulting baud rate is 1/16 of the clocking rate selected through the BRG circuit. The maximum baud rate generated using the BRG is 625 kbaud.

In the Synchronous Mode data is transmitted on the rising edge and received on the falling edge of the external clock. Although the data is transmitted and received synchronously, it is still contained within an asynchronous frame; i.e., a start bit, parity bit (if selected) and stop bit(s) are still present.

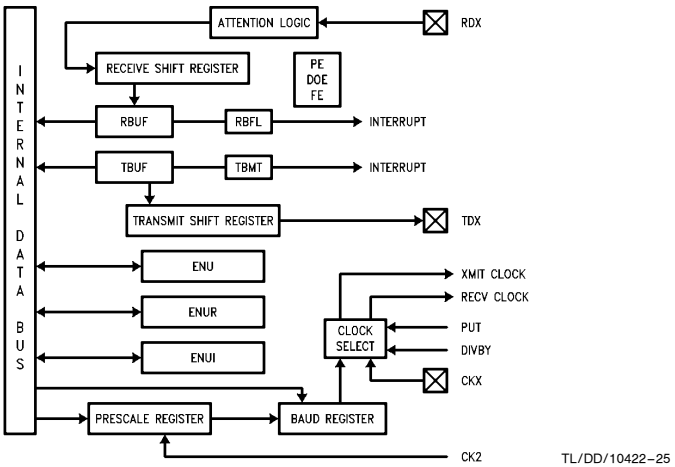

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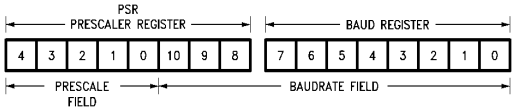
FIGURE 16. UART Block Diagram



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UART Baud Rate Generator (BRG) Registers PSR and BAUD

UART Attention Mode

The HPC46400E UART features an Attention Mode of operation. This mode of operation enables the HPC46400E to be networked with other processors. Typically in such environments, the messages consist of addresses and actual data. Addresses are specified by having the ninth bit in the data frame set to 1. Data in the message is specified by having the ninth bit in the data frame reset to 0.

The UART monitors the communication stream looking for addresses. When the data word with the ninth bit set is received, the UART signals the HPC46400E with an interrupt. The processor then examines the content of the receiver buffer to decide whether it has been addressed and whether to accept subsequent data.

Programmable Serial Decoder Interface

The programmable serial decoder interface allows the two HDLC channels to be used with devices employing several popular Time Division Multiplexing (TDM) serial protocols for point-to-point and multipoint data exchanges. These protocols combine the 'B' and 'D' channels onto common pins—received data, transmit data, clock and Sync, which normally occurs at an 8 KHz rate and provides framing for the particular protocol.

The decoder uses the serial link clock and Sync signals to generate internal enables for the 'D' and 'B' channels, thereby allowing the HDLC channels to access the appropriate channel data from the multiplexed link.

Additionally, 64 kbit/s to 56 kbits/s rate adaptation can be done using the Serial Decoder generated enable signals B1 or B2. The rate adaption to 56 kbits/s is accomplished by using only the first 7 bits of each B channel time slot for each TDM frame. The transmitter will insert a ''1'' in the eighth bit of each frame. The receiver will only receive the first seven data bits and skip the eighth bit. See *Figure 17* 65 kbit/56 kbit Rate Adaption Timing Diagram.

HDLC Channel Description

HDLC/DMA Structure

HDLC 1		HDLC 2	
HDLC1 Receive	HDLC1 Transmit	HDLC2 Receive	HDLC2 Transmit
DMAR1	DMAT1	DMAR2	DMAT2

GENERAL INFORMATION

Both HDLC channels on the HPC46400E are identical and operate up to 4.65 Mbps. When used in an ISDN Basic Rate access application, HDLC channel #1 has been designated for use with the 16 kbps D-channel or either B channel and HDLC #2 can be used with either of the 64 kbps B-channels. If the 'D' and 'B' channels are present on a common serial link, the programmable serial decoder interface generates the necessary enable signals needed to access the D and B channel data.

There are two sources for the receive and transmit channel enable signals. They can be internally generated from the serial decoder interface or they can be externally enabled.

LAPD, the Link Access Protocol for the D channel is derived from the X.25 packet switching LAPB protocol. LAPD specifies the procedure for a terminal to use the D channel for the transfer of call control or user-data information. The procedure is used in both point-to-point and point-to-multipoint configurations. On the HPC46400E, the HDLC controller contains user programmable features that allow for the efficient processing of LAPD Information.

HDLC Channel Pin Description

Each HDLC channel has the following pins associated with it.

HCK — HDLC Channel Clock Input Signal.

RX — Receive Serial Data Input. Data latched on the negative HCK edge.

REN/RHCK — HDLC Channel Receiver Enable Input/Receiver Clock Input.

TEN — HDLC Channel Transmitter Enable Input.

TX — Transmit Serial Data Output. Data clocked out on the positive HCK edge. Data (not including CRC) is sent LSB first. TRI-STATE when transmitter not enabled.

CFLG1 — Closing Flag output for Channel 1.

HDLC Functional Description

TRANSMITTER DESCRIPTION

Data is transferred from external memory through the DMA controller into the transmit buffer register, from which it is loaded into a 8-bit serial shift register. The CRC is computed and appended to the frame prior to the closing flag being transmitted. Data is output at the TX output pin. If no further transmit commands are given the transmitter sends out continous flags, aborts, or the idle pattern as selected by the control register.

An interrupt is generated when the DMA has transferred the last byte from RAM to the HDLC channel for a particular message or on a transmit error condition. An associated transmit status register will contain the status information indicating the specific interrupt source.

To support transmitting data packets at an ''R'' interface for V.120 in synchronous UI mode, to support the use of the HPC in test equipment, or to support proprietary CRC algorithms the transmitter has the option of preventing the transmitting of the hardware generated CRC bytes.

TRANSMITTER FEATURES

Interframe fill: the transmitter can send either continuous '1's or repeated flags or aborts between the closing flag of one packet and the opening flag of the next. When the CPU commands the transmitter to open a new frame, the interframe fill is terminated immediately.

Abort: the abort sequence, a zero followed by seven ones, will be immediately sent on command from the CPU or on an underrun condition in the DMA.

Bit/Byte boundaries: The message length between packet headers may have any number of bits and is not confined to an integral number of bytes. Three bits in the control register are used to indicate the number of valid bits in the last byte. These bits are loaded by the users software.

RECEIVER DESCRIPTION

Data is input to the receiver on the RX pin. The receive clock can be externally input at either the HCK pin or the REN/RHCK pin.

Incoming data is routed through one of several paths depending on whether it is the flag, data, or CRC.

Once the receiver is enabled it waits for the opening flag of the incoming frame, then starts the zero bit deletion, ad-

HDLC Functional Description (Continued)

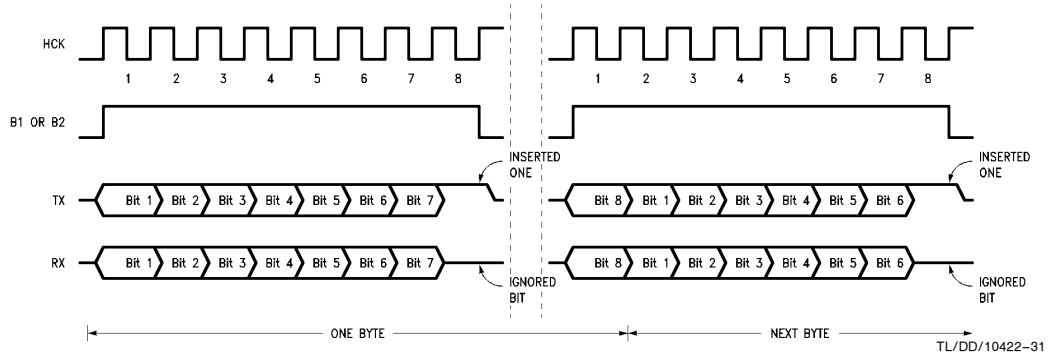

FIGURE 17. 64 kbit/56 kbit Rate Adaption Timing Diagram

dressing handling and CRC checking. All data between the flags is shifted through two 8-bit serial shift registers before being loaded into the buffer register. The user programmable address register values are compared to the incoming data while it resides in the shift registers. If an address match occurs or if operating in the transparent address recognition mode, the DMA channel is signaled that attention is required and the data is transferred by it to external memory. Appropriate interrupts are generated to the CPU on the reception of a complete frame, or on the occurance of a frame error.

The receive interrupt, in conjunction with status data in the control registers allows interrupts to be generated on the following conditions—frame length error, CRC error, receive error, abort and receive complete.

To support V.120 UI data packets at the ''R'' interface, proprietary CRC algorithms, and test equipment the two bytes preceding the closing flag (usually the CRC bytes) will be loaded into registers. The two bytes can then be read by the CPU and placed into memory. The DMA address pointers used for that particular message will already contain the address that the first byte should be placed into.

RECEIVER FEATURES

Flag sharing: the closing flag of one packet may be shared as the opening flag of the next. Receiver will also be able to share a zero between flags—011111101111110 is a valid two flag sequence for receive (not transmit).

Interframe fill: the receiver automatically accepts either repeated flags, repeated aborts, or all '1's as the interframe fill.

Idle: Reception of successive flags as the interframe fill sequence to be signaled to the user by setting the Flag bit in the Receiver Status register.

Short Frame Rejection: Reception of greater than 2 bytes but less than 4 bytes between flags will generate a frame error, terminating reception of the current frame and setting the Frame Error (FER) status bit in the Receive Control and Status register. Reception of less than 2 bytes will be ignored.

Abort: the 7 '1's abort sequence will be immediately recognized and will cause the receiver to reinitialize and return to searching the incoming data for an opening flag. Reception of the abort will cause the abort status bit in the Interrupt Error Status register to be set and will signal an End of Message (EOMR).

Bit/Byte boundaries: The message length between packet headers may have any number of bits and it is not confined to an integral number of bytes. Three bits in the status register are used to indicate the number of valid bits in the last byte.

Address Recognition: Two user programmable bytes are available to allow frame address recognition on the two bytes immediately following the opening flag. When the received address matches the programmed value(s), the frame is passed through to the DMA channel. If no match occurs, the received frame address information is disregarded and the receiver returns to searching for the next opening flag and the address recognition process starts anew.

Support is provided to allow recognition of the Broadcast address. Additionally, a transparent mode of operation is available where no address decoding is done.

HDLC INTERRUPT CONDITIONS

The end of message interrupt (EOM) indicates that a complete frame has been received or transmitted by the HDLC controller. Thus, there are four separate sources for this interrupt, two each from each HDLC channel. The Message Control Register contains the pending bits for each source.

HDLC ERROR DETECTION

The HDLC/DMA detects several error conditions and reports them in the two Error Status Registers. These conditions are a DMA transmitter underrun, a DMA receiver overrun, a CRC error, a frame too long, a frame too short, and an aborted message.

HDLC CHANNEL CLOCK

Each HDLC channel uses the falling edge of the clock to sample the receive data. Outgoing transmit data is shifted out on the rising edge of the external clock. The maximum data rate when using the externally provided clocks is 4.65 Mb/s.

The receiver/transmitter pair can share a single clock input to save I/O pins, or the inputs can be separated to allow different receive and transmit clocks. This feature allows the receiver and transmitter to operate at different frequencies or enables them to each be synchronized to different parts of the user's system.

CYCLIC REDUNDACY CHECK

There are two standard CRC codes used in generating the 16-bit Frame Check Sequence (FCS) that is appended to the end of the data frame. Both codes are supported and

HDLC Functional Description (Continued)

the user selects the error checking code to be used through software control (HDLC control reg). The two error checking polynomials available are:

(1) CRC-16 ($x^{16} + x^{15} + x^2 + 1$)

(2) CCITT CRC ($x^{16} + x^{12} + x^5 + 1$)

SYNCHRONOUS BYPASS MODE

When the BYPAS bit is set in the HDLC control register, all HDLC framing/formatting functions for the specified HDLC channel are disabled.

This allows byte-oriented data to be transmitted and received synchronously thus ''bypassing'' the HDLC functions.

LOOP BACK OPERATIONAL MODE

The user has the ability, by setting the appropriate bit in the register to internally route the transmitter output to the receiver input, and to internally route the RX pin to the TX pin.

DMA Controller

GENERAL INFORMATION

The HPC46400E uses Direct Memory Access (DMA) logic to facilitate data transfer between the 2 full Duplex HDLC channels and external packet RAM. There are four DMA channels to support the four individual HDLC channels. Control of the DMA channels is accomplished through registers which are configured by the CPU. These control registers define specific operation of each channel and changes are immediately reflected in DMA operation. In addition to individual control registers, global control bits (MSS and MSSC in Message Control Register) are available so that the HDLC channels may be globally controlled.

The DMA issues a bus request to the CPU when one or more of the individual HDLC channels request service. Upon receiving a bus acknowledge from the CPU, the DMA completes all requests pending and any requests that may have occurred during DMA operation before returning control to the CPU. If no further DMA transfers are pending, the DMA relinquishes the bus and the CPU can again initiate a bus cycle.

Four memory expansion bits have been added for each of the four channels to support data transfers into the expanded memory bank areas.

The DMA has priority logic for servicing DMA requests. The priorities are:

1st priority . . . . . Receiver channel 1

2nd priority . . . . . Transmit channel 1

3rd priority . . . . . Receive channel 2

4th priority . . . . . Transmit channel 2

RECEIVER DMA OPERATION

The receiver DMA consists of a shift register and two buffers. A receiver DMA operation is initiated by the buffer registers. Once a byte has been placed in a buffer register from the HDLC, it generates a request and upon obtaining control of the bus, the DMA places the byte in external memory.

RECEIVER REGISTERS

All the following registers are Read/Write

A. Frame Length Register

This user programmable 16-bit register contains the maximum number of bytes to be placed in a data ''block''. If this number is exceeded, a Frame Too Long error is generated. DMA is stopped to prevent memory from being overwritten, however the receiver continues until the closing flag is received in order to check the CRC.

B. CNTRL ADDR 1
DATA ADDR 1
CNTRL ADDR 2
DATA ADDR 2

For split frame operation, the CNTRL ADDR register contains the external memory address where the Frame Header (Control & Address fields) are to be stored and the DATA ADDR register contains an equivalent address for the Information field.

For non-split frame operation, the CNTRL and DATA ADDR registers each contain the external memory address for entire frames.

TRANSMITTER DMA OPERATION

The transmitter DMA consists of a shift register and two buffers. A transmitter DMA cycle is initiated by the TX data buffers. The TX data buffers generate a request when either one is empty and the DMA responds by placing a byte in the buffer. The HDLC transmitter can then accept the byte to send when needed, upon which the DMA will issue another request, resulting in a subsequent DMA cycle.

TRANSMITTER REGISTERS

The following registers are Read/Write:

FIELD ADDRESS 1
BYTE COUNT 1
FIELD ADDRESS 2
BYTE COUNT 2

Field Address 1 and Field Address 2 are starting addresses of blocks of information to be transmitted.

Byte Count 1 and Byte Count 2 are the number of bytes in the block to be transmitted.

Shared Memory Support

Shared memory access provides a rapid technique to exchange data. It is effective when data is moved from a peripheral to memory or when data is moved between blocks of memory. A related area where shared memory access proves effective is in multiprocessing applications where two CPUs share a common memory block. The HPC46400E supports shared memory access with two pins. The pins are the RDY/$\overline{\text{HLD}}$ input pin and the $\overline{\text{HLDA}}$ output pin. The user can software select either the Hold or Ready function on the RDY/$\overline{\text{HLD}}$ pin by the state of a control bit. The $\overline{\text{HLDA}}$ output must be selected as the $\overline{\text{HLDA}}$ output on pin B7 by software.

The host uses DMA to interface with the HPC46400E. The host initiates a data transfer by activating the $\overline{\text{HLD}}$ input of the HPC46400E. In response, the HPC46400E places its system bus in a TRI-STATE Mode, freeing it for use by the host. The host waits for the acknowledge signal ($\overline{\text{HLDA}}$) from the HPC46400E indicating that the sytem bus is free. On receiving the acknowledge, the host can rapidly transfer data into, or out of, the shared memory by using a conventional DMA controller. Upon completion of the message transfer, the host removes the HOLD request and the HPC46400E resumes normal operations. See *Figure 18* (HPC46400E shared Memory Using HOLD).

An alternate approach is to use the Ready function available on either the RDY/$\overline{\text{HLD}}$ pin or the INT4/RDY pin. See *Figure 19* (HPC46400E Shared Memory Using READY). This technique is often required when the HPC is sharing memory over a system backplane bus.

Shared Memory Support (Continued)

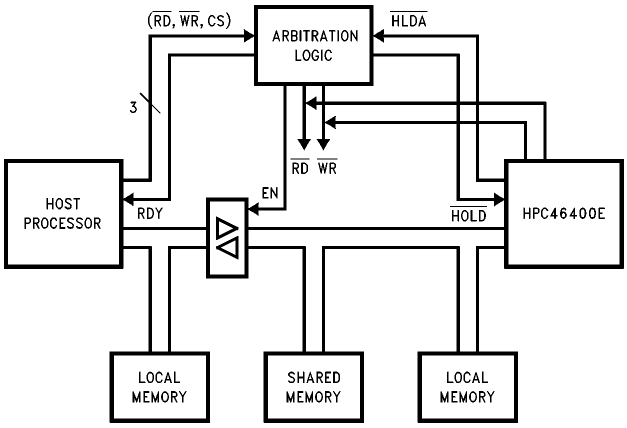

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FIGURE 18. HPC46400E Shared Memory Using HOLD

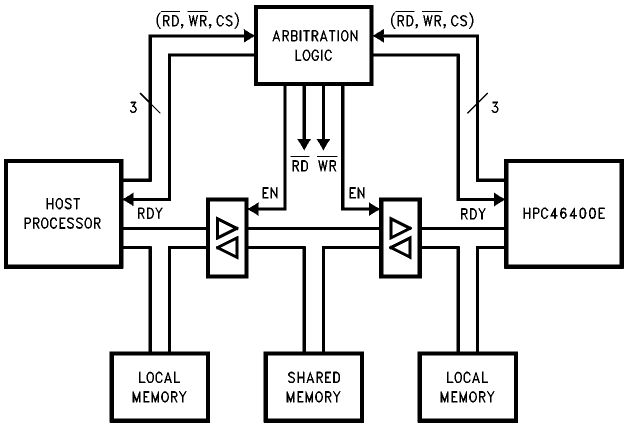

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FIGURE 19. HPC46400E Shared Memory Using READY

Memory

The HPC46400E has been designed to offer flexibility in memory usage. A total address space of 64 kbytes can be addressed with 256 bytes of RAM available on the chip itself.

Program memory addressing is accomplished by the 16-bit program counter on a byte basis. Memory can be addressed directly by instructions or indirectly through the B, X and SP registers. Memory can be addressed as words or bytes. Words are always accessed on even-byte boundaries. The HPC46400E uses memory-mapped organization to support registers, I/O and on-chip peripheral functions.

The HPC46400E memory address space extends to 64 kbytes and registers and I/O are mapped as shown in Table II.

Extended Memory Addressing

If more than 64k of addressing is desired in a HPC46400E system, on board bank select circuitry is available that allows four I/O lines of Port B (B8, B9, B13, B14) to be used in extending the address range. This gives the user a main routine area of 32k and 16 banks of 32k each for subroutine and data, thus getting a total of 536.5k of memory.

Note: If all four lines are not needed for memory expansion, the unused lines can be used as general purpose inputs.

The Extended Memory Addressing mode is entered by setting the EMA control bit in the Message Control Register. If this bit is not set, the port B lines (B8, B9, B13, B14) are available as general purpose I/O or synchronous outputs as selected by the BFUN register.

The main memory area contains the interrupt vectors & service routines, stack memory, and common memory for the bank subroutines to use. The 16 banks of memory can contain program or data memory (note: since the on chip resources are mapped into addresses 0000-01FF, the first 512 bytes of each bank are not usable, actual available memory is 536.5k).

TABLE II. Memory Map

FFFF–FFF0 FFEF–FFD0	Interrupt Vectors JSRP Vectors	
FFCF–FFCE : : 0201–0200	External Expansion	USER MEMORY
01FF–01FE : : 01C1–01C0	On Chip RAM	USER RAM
01BC 01BA 01B8 01B6 01B4 01B2 01B0	CRC Byte 2 CRC Byte 1 Error Status Receiver Status Cntrl Recr Addr Comp Reg 2 Recr Addr Comp Reg 1	HDLC # 2
01AC 01AA 01A8 01A6 01A4 01A2 01A0	CRC Byte 2 CRC Byte 1 Error Status Receiver Status Cntrl Recr Addr Comp Reg 2 Recr Addr Comp Reg 1	HDLC # 1
0195–0194	WATCHDOG Register	WATCHDOG Logic
0193–0192 0191–0190 018F–018E 018D–018C 018B–018A 0189–0188 0187–0186 0185–0184 0183–0182 0181–0180	T0CON Register TMMODE Register DIVBY Register T3 Timer R3 Register T2 Timer R2 Register I2CR Register/ R1 I3CR Register/ T1 I4CR Register	Timer Block T0–T3
017F–017E 017D–017C	Baud Counter Baud Register	UART Timer
0179–0178 0177–0176 0175–0174 0173–0172 0171–0170	Byte Count 2 Field Addr 2 Byte Count 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 2 (Xmit)
016B–016A 0169–0168 0167–0166 0165–0164 0163–0162 0161–0160	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 2 (Recv)
0159–0158 0157–0156 0155–0154 0153–0152 0151–0150	# Bytes 2 Field Addr 2 # Bytes 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 1 (Xmit)
014B–014A 0149–0148 0147–0146 0145–0144 0143–0142 0141–0140	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 1 (Recv)
012C 012A 0128 0126 0124 0122 0120	Baud PSR - Prescaler ENUR Register TBUF Register RBUF Register ENUI Register ENU Register	UART
0110 010E 010C 010A 0108 0106 0104 0102 0100	FEXT Register Port R Pins DIR R Register Port R Data Register Message System Configuration Serial Decoder/Enable Configuration Reg Message Pending Message System Control Port D Input	PORTS R & D
00F5–00F4 00F3–00F2 00E6 00E3–00E2	BFUN Register DIR B Register Chip Revision Register Port B	PORT B
00DD–00DC 00D8 00D6 00D4 00D2 00D0	Halt Enable Register Port I Input Register SIO Register IRCD Register IRPD Register ENIR Register	PORT CONTROL & INTERRUPT CONTROL REGISTERS
00CF–00CE 00CD–00CC 00CB–00CA 00C9–00C8 00C7–00C6 00C5–00C4 00C3–00C2 00C0	X Register B Register K Register A Register PC Register SP Register (Reserved) PSW Register	HPC CORE REGISTERS
00BF–00BE : : 0001–0000	On Chip RAM	USER RAM

Note: All unused addresses are reserved by National Semiconductor

Design Considerations

Designs using the HPC family of 16-bit high speed CMOS microcontrollers need to follow some general guidelines on usage and board layout.

Floating inputs are a frequently overlooked problem. CMOS inputs have extremely high impedance and, if left open, can float to any voltage possibly causing internal devices to go into active mode and draw DC current. You should thus tie unused inputs to V_{CC} or ground, either through a resistor or directly. Unlike the inputs, unused outputs should be left floating to allow the output to switch without drawing any DC current.

To reduce voltage transients, keep the supply line's parasitic inductances as low as possible by reducing trace lengths, using wide traces, ground planes, and by decoupling the supply with bypass capacitors. In order to prevent additional voltage spiking, this local bypass capacitor must exhibit low inductive reactance. You should therefore use high frequency ceramic capacitors and place them very near the IC to minimize wiring inductance.

- Keep V_{CC} bus routing short. When using double sided or multilayer circuit boards, use ground plane techniques.
- Keep ground lines short, and on PC boards make them as wide as possible, even if trace width varies. Use separate ground traces to supply high current devices such as relay and transmission line drivers.
- In systems mixing linear and logic functions and where supply noise is critical to the analog components' performance, provide separate supply buses or even separate supplies.
- When using local regulators, bypass their inputs with a tantalum capacitor of at least 1 μF and bypass their outputs with a 10 μF to 50 μF tantalum or aluminum electrolytic capacitor.
- If the system uses a centralized regulated power supply, use a 10 μF to 20 μF tantalum electrolytic capacitor or a 50 μF to 100 μF aluminum electrolytic capacitor to decouple the V_{CC} bus connected to the circuit board.
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) per every two to five packages, and 100 nF for every 10 packages. You can group these capacitances, but it's more effective to distribute them among the ICs. If the design has a fair amount of synchronous logic with outputs that tend to switch simultaneously, additional decoupling might be advisable. Octal flip-flop and buffers in bus-oriented circuits might also require more decoupling. Note that wire-wrapped circuits can require more decoupling than ground plane or multilayer PC boards.

A recommended crystal oscillator circuit to be used with the HPC is shown in *Figure 20*. See table for recommended component values. The recommended values given in the table below have yielded consistent results and are made to match a crystal with a 20 pF load capacitance, with some small allowance for layout capacitance.

A recommended layout for the oscillator network should be as close to the processor as physically possible, entirely within 1″ distance. This is to reduce lead inductance from long PC traces, as well as interference from other components, and reduce trace capacitance. The layout should contain a large ground plane either on the top or bottom surface of the board to provide signal shielding, and a convenient location to ground both the HPC, and the case of the crystal.

It is very critical to have an extremely clean power supply for the HPC crystal oscillator. Ideally one would like a V_{CC} and ground plane that provide low inductance power lines to the chip. The power planes in the PC board should be decoupled with three decoupling capacitors as close to the chip as possible. A 1.0 μF, a 0.1 μF, and a 0.001 μF dipped mica or ceramic cap mounted as close to the HPC as is physically possible on the board, using the shortest leads, or surface mount components. This should provide a stable power supply, and noiseless ground plane which will vastly improve the performance of the crystal oscillator network.

HPC Oscillator Table

XTAL Frequency (MHz)	R1 (Ω)
$\leq$2	1500
4	1200
6	910
8	750
10	600
12	470
14	390
16	300
18	220
20	180

R_F = 3.3 MΩ

C1 = 27 pF

C2 = 33 pF

XTAL Specifications: The crystal used was an M-TRON Industries MP-1 Series XTAL ''AT'' cut parallel resonant.

C_L = 18 pF

Series Resistance is

40Ω @ 10 MHz

600Ω @ 2 MHz

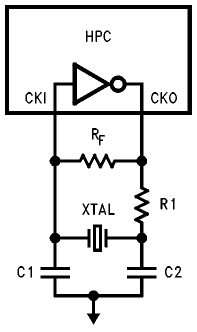

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FIGURE 20. Recommended Crystal Circuit

HPC46400E CPU

The HPC46400E CPU has a 16-bit ALU and six 16-bit registers.

Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and can do 16-bit add, subtract and shift or logic AND, OR and exclusive OR in one timing cycle. The ALU can also output the carry bit to a 1-bit C register.

Accumulator (A) Register

The 16-bit A register is the source and destination register for most I/O, arithmetic, logic and data memory access operations.

Address (B and X) Registers

The 16-bit B and X registers can be used for indirect addressing. They can automatically count up or down to sequence through data memory.

Boundary (K) Register

The 16-bit K register is used to set limits in repetitive loops of code as register B sequences through data memory.

Stack Pointer (SP) Register

The 16-bit SP register is the stack pointer that addresses the stack. The SP register is incremented by two for each push or call and decremented by two for each pop or return. The stack can be placed anywhere in user memory and be as deep as the available memory permits.

Program (PC) Register

The 16-bit PC register addresses program memory.

Addressing Modes

ADDRESSING MODES—ACCUMULATOR AS DESTINATION

Register Indirect

This is the ''normal'' mode of addressing for the HPC46400E (instructions are single-byte). The operand is the memory addressed by the B register (or X register for some instructions).

Direct

The instruction contains an 8-bit or 16-bit address field that directly points to the memory for the operand.

Indirect

The instruction contains an 8-bit address field. The contents of the WORD addressed points to the memory for the operand.

Indexed

The instruction contains an 8-bit address field and an 8- or 16-bit displacement field. The contents of the WORD addressed is added to the displacement to get the address of the operand.

Immediate

The instruction contains an 8-bit or 16-bit immediate field that is used as the operand.

Register Indirect (Auto Increment and Decrement)

The operand is the memory addressed by the X register. This mode automatically increments or decrements the X register (by 1 for bytes and by 2 for words).

Register Indirect (Auto Increment and Decrement) with Conditional Skip

The operand is the memory addressed by the B register. This mode automatically increments or decrements the B register (by 1 for bytes and by 2 for words). The B register is then compared with the K register. A skip condition is generated if B goes past K.

ADDRESSING MODES—DIRECT MEMORY AS DESTINATION

Direct Memory to Direct Memory

The instruction contains two 8- or 16-bit address fields. One field directly points to the source operand and the other field directly points to the destination operand.

Immediate to Direct Memory

The instruction contains an 8- or 16-bit address field and an 8- or 16-bit immediate field. The immediate field is the operand and the direct field is the destination.

Double Register Indirect using the B and X Registers

Used only with Reset, Set and IF bit instructions; a specific bit within the 64 kbyte address range is addressed using the B and X registers. The address of a byte of memory is formed by adding the contents of the B register to the most significant 13 bits of the X register. The specific bit to be modified or tested within the byte of memory is selected using the least significant 3 bits of register X.

HPC Instruction Set Description

Mnemonic	Description	Action	
ARITHMETIC INSTRUCTIONS			
ADD	Add	MA + Meml ⟶ MA	carry ⟶ C
ADDS	Add short imm8	MA + imm8 ⟶ MA	carry ⟶ C
ADC	Add with carry	MA + Meml + C ⟶ MA	carry ⟶ C
DADC	Decimal add with carry	MA + Meml + C ⟶ MA (Decimal)	carry ⟶ C
SUBC	Subtract with carry	MA − Meml + C ⟶ MA	carry ⟶ C
DSUBC	Decimal subtract w/carry	MA − Meml + C ⟶ MA (Decimal)	carry ⟶ C
MULT	Multiply (unsigned)	MA*Meml ⟶ MA & X, 0 ⟶ K, 0 ⟶ C	
DIV	Divide (unsigned)	MA/Meml ⟶ MA, rem. ⟶ X, 0 ⟶ K, 0 ⟶ C	
DIVD	Divide Double Word (unsigned)	(x8 MA)/Meml ⟶ MA, rem ⟶ X, 0 ⟶ K	carry ⟶ C
IFEQ	If equal	Compare MA & Meml, Do next if equal	
IFGT	If greater than	Compare MA & Meml, Do next if MA ⟶ Meml	
AND	Logical and	MA and Meml ⟶ MA	
OR	Logical or	MA or Meml ⟶ MA	
XOR	Logical exclusive-or	MA xor Meml ⟶ MA	
MEMORY MODIFY INSTRUCTIONS			
INC	Increment	Mem + 1 ⟶ Mem	
DECSZ	Decrement, skip if 0	Mem −1 ⟶ Mem, Skip next if Mem = 0	
BIT INSTRUCTIONS			
SBIT	Set bit	1 ⟶ Mem.bit (bit is 0 to 7 immediate)	
RBIT	Reset bit	0 ⟶ Mem.bit	
IFBIT	If bit	If Mem.bit is true, do next instr.	
MEMORY TRANSFER INSTRUCTIONS			
LD	Load	Meml ⟶ MA	
	Load, incr/decr X	Mem(X) ⟶ A, X ±1 (or 2) ⟶ X	
ST	Store to Memory	MA ⟶ Mem	
X	Exchange	A ⟷ Mem; Mem ⟷ Mem	
	Exchange, incr/decr X	A ⟷ Mem(X), X ±1 (or 2) ⟶ X	
PUSH	Push Memory to Stack	W ⟶ W(SP), SP + 2 ⟶ SP	
POP	Pop Stack to Memory	SP − 2 ⟶ SP, W(SP) ⟶ W	
LDS	Load A, incr/decr B, Skip on condition	Mem(B) ⟶ A, B ±1 (or 2) ⟶ B, Skip next if B greater/less than K	
XS	Exchange, incr/decr B, Skip on condition	Mem(B) ⟷ A,B ±1 (or 2) ⟶ B, Skip next if B greater/less than K	
REGISTER LOAD IMMEDIATE INSTRUCTIONS			
LD A	Load A immediate	imm ⟶ A	
LD B	Load B immediate	imm ⟶ B	
LD K	Load K immediate	imm ⟶ K	
LD X	Load X immediate	imm ⟶ X	
LD BK	Load B and K immediate	imm ⟶ B,imm ⟶ K	
ACCUMULATOR AND C INSTRUCTIONS			
CLR A	Clear A	0 ⟶ A	
INC A	Increment A	A + 1 ⟶ A	
DEC A	Decrement A	A − 1 ⟶ A	
COMP A	Complement A	1's complement of A ⟶ A	
SWAP A	Swap nibbles of A	A15:12 ⟵ A11:8 ⟵ A7:4 ⟷ A3:0	
RRC A	Rotate A right thru C	C ⟶ A15 ⟶ . . . ⟶ A0 ⟶ C	
RLC A	Rotate A left thru C	C ⟵ A15 ⟵ . . . ⟵ A0 ⟵ C	
SHR A	Shift A right	0 ⟶ A15 ⟶ . . . ⟶ A0 ⟶ C	
SHL A	Shift A left	C ⟵ A15 ⟵ . . . ⟵ A0 ⟵ 0	
SC	Set C	1 ⟶ C	
RC	Reset C	0 ⟶ C	
IFC	IF C	Do next if C = 1	
IFNC	IF not C	Do next if C = 0	

HPC Instruction Set Description (Continued)

Mnemonic	Description	Action
TRANSFER OF CONTROL INSTRUCTIONS		
JSRP	Jump subroutine from table	PC ⟶ W(SP),SP + 2 ⟶ SP W(table #) ⟶ PC
JSR	Jump subroutine relative	PC ⟶ W(SP),SP + 2 ⟶ SP,PC + # ⟶ PC (# is +1024 to −1023)
JSRL	Jump subroutine long	PC ⟶ W(SP),SP + 2 ⟶ SP,PC + # ⟶ PC
JP	Jump relative short	PC + # ⟶ PC(# is +32 to −31)
JMP	Jump relative	PC + # ⟶ PC(# is +256 to −255)
JMPL	Jump relative long	PC + # ⟶ PC
JID	Jump indirect at PC + A	PC + A + 1 ⟶ PC
JIDW		then Mem(PC) + PC ⟶ PC
NOP	No Operation	PC ⟵ PC + 1
RET	Return	SP − 2 ⟶ SP,W(SP) ⟶ PC
RETS	Return then skip next	SP − 2 ⟶ SP,W(SP) ⟶ PC, & skip
RETI	Return from interrupt	SP − 2 ⟶ SP,W(SP) ⟶ PC, interrupt re-enabled

Note: W is 16-bit word of memory
MA is Accumulator A or direct memory (8-bit or 16-bit)
Mem is 8-bit byte or 16-bit word of memory
MemI is 8-bit or 16-bit memory or 8-bit or 16-bit immediate data
imm is 8-bit or 16-bit immediate data

Memory Usage

For information on memory usage and instruction timing please refer to the HPC46400E User's Manual (See page 25 for ordering information).

Code Efficiency

The HPC46400E has been designed to be extremely code-efficient. The HPC46400E looks very good in all the standard coding benchmarks; however, it is not realistic to rely only on benchmarks. Many large jobs have been programmed onto the HPC46400E, and the code savings over other popular microcontrollers has been considerable.

Reasons for this saving of code include the following:

SINGLE BYTE INSTRUCTIONS

The majority of instructions on the HPC46400E are single-byte. There are two especially code-saving instructions:

JP is a 1-byte jump. True, it can only jump within a range of plus or minus 32, but many loops and decisions are often within a small range of program memory. Most other micros need 2-byte instructions for any short jumps.

JSRP is a 1-byte call subroutine. The user makes a table of his 16 most frequently called subroutines and these calls will only take one byte. Most other micros require two and even three bytes to call a subroutine. The user does not have to decide which subroutine addresses to put into his table; the assembler can give him this information.

EFFICIENT SUBROUTINE CALLS

The 2-byte JSR instructions can call any subroutine within plus or minus 1k of program memory.

MULTIFUNCTION INSTRUCTIONS FOR DATA MOVEMENT AND PROGRAM LOOPING

The HPC46400E has single-byte instructions that perform multiple tasks. For example, the XS instruction will do the following:

1. Exchange A and memory pointed to by the B register
2. Increment or decrement the B register
3. Compare the B register to the K register
4. Generate a conditional skip if B has passed K

The value of this multipurpose instruction becomes evident when looping through sequential areas of memory and exiting when the loop is finished.

BIT MANIPULATION INSTRUCTIONS

Any bit of memory, I/O or registers can be set, reset or tested by the single byte bit instructions. The bits can be addressed directly or indirectly. Since all registers and I/O are mapped into the memory, it is very easy to manipulate specific bits to do efficient control.

DECIMAL ADD AND SUBTRACT

This instruction is needed to interface with the decimal user world.

It can handle both 16-bit words and 8-bit bytes.

The 16-bit capability saves code since many variables can be stored as one piece of data and the programmer does not have to break his data into two bytes. Many applications store most data in 4-digit variables. The HPC46400E supplies 8-bit byte capability for 2-digit variables and literal variables.

MULTIPLY AND DIVIDE INSTRUCTIONS

The HPC46400E has 16-bit multiply, 16-bit by 16-bit divide, and 32-bit by 16-bit divide instructions. This saves both code and time. Multiply and divide can use immediate data or data from memory. The ability to multiply and divide by immediate data saves code since this function is often needed for scaling, base conversion, computing indexes of arrays, etc.

Part Selection

The HPC family includes devices with many different options and configurations to meet various application needs. The number HPC46400E has been generally used throughout this datasheet to represent the whole family of parts. The following chart explains how to order various options available when ordering HPC family members.

Note: All options may not currently be available.

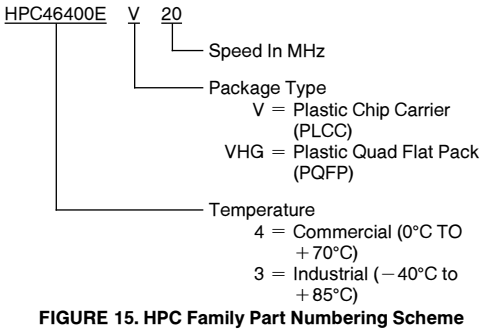


FIGURE 15. HPC Family Part Numbering Scheme

EXAMPLES

HPC46400EV20—Commercial temp (0° to +70°C), PLCC

HPC36400EV20—Industrial temp (−40°C to +85°C), PLCC

Development Support

HPC MICROCONTROLLER DEVELOPMENT SYSTEM

The HPC microcontroller development system is an in-system emulator (ISE) designed to support the entire family of HPC Microcontrollers. The complete package of hardware and software tools combined with a host system provides a powerful system for design, development and debug of HPC based designs. Software tools are available for IBM®, PC-AT® (MS-DOS, PC-DOS) and for UNIX® based multiuser Sun SPARCstation (SunOS™).

The stand alone unit comes complete with a power supply and external emulation POD. This unit can be connected to various host systems through an RS-232 link. The software package includes an ANSI compatible C-Compiler, Linker, Assembler and librarian package. Source symbolic debug capability is provided through a user friendly MS-windows 3.0 interface for IBM PC-AT environment and through a line debugger under Sunview for Sun SPARCstations.

The ISE provides fully transparent in-system emulation at speeds up to 20 MHz 1 waitstate. A 2K word (48-bit wide) trace buffer gives trace trigger and non intrusive monitoring of the system. External triggering is also available through an external logic interface socket on the POD. Comprehensive on-line help and diagnostics features reduce user's design and debug time. 8 hardware breakpoints (Address/range), 64 kbytes of user memory, and break on external events are some of the other features offered.

Hewlett Packard model HP64775 Emulator/Analyzer providing in-system emulation for up to 30 MHz 1 waitstate is also available. Contact your local sales office for technical details and support.

Development Tools Selection Table

Product	Order Part Number	Description	Included	Manual Number
HPC46400E	HPC-DEV-ISE2	HPC In-System Emulator	HPC MDS User's Manual HPC46400E User's Manual	420420184-001 420420213-001
	HPC-DEV-ISE2-E	HPC In-System Emulator for Europe and South East Asia		
	HPC-DEV-IBMA	Assembler/Linker/ Library Package for IBM PC-AT	HPC Assembler/Linker/ Librarian User's Manual for IBM PC-AT	424410836-001
	HPC-DEV-IBMC	C Compiler/Assembler/ Linker/Library Package for IBM PC-AT	HPC C Compiler User's Manual HPC Assembler/Linker/Librarian User's Manual	424410883-001 424410836-001
	HPC-DEV-WDBC	Source Symbolic Debugger for IBM PC-AT C Compiler/Assembler/Linker Library Package for IBM PC-AT	HPC Source Symbolic Debugger User's Manual HPC C Compiler User's Manual HPC Assembler/Linker/Librarian User's Manual	424420189-001 424410883-001 424410836-001
	HPC-DEV-SUNC	C Compiler/Assembler/Linker Library Package for Sun SPARCstation	HPC C Compiler User's Manual HPC Assembler/Linker/Library User's Manual	424410883-001 424410836-001
	HPC-DEV-SUNDB	Source/Symbolic Debugger C Compiler/Assembler/Linker Library Package for Sun SPARCstation	Source/Symbolic Debugger User's Manual HPC C Compiler User's Manual HPC Assembler/Linker/Library User's Manual	424420189-001 424410883-001 424410836-001

Development Support (Continued)

Development Tools Selection Table (Continued)

Product	Order Part Number	Description	Included	Manual Number
Complete System				
HPC46400E	HPC-DEV-SYS2	HPC In-System Emulator with C Compiler, Assembler/Linker/Library and Source Symbolic Debugger	HPC Microcontroller Development System User's Manual	420420184-001
	HPC-DEV-SYS2-E	Same for Europe and South East Asia	HPC 46400E User's Manual	420420213-001
			C-Compiler Manual	424410883-001
			Assembler Manual	424410836-001
			Debugger User's Manual	424420189-001

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications Group. Dial-A-Helper is an electronic bulletin board information system and additionally, provides the capability of remotely accessing the development system at a customer site.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities can be found. The minimum requirement for accessing Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

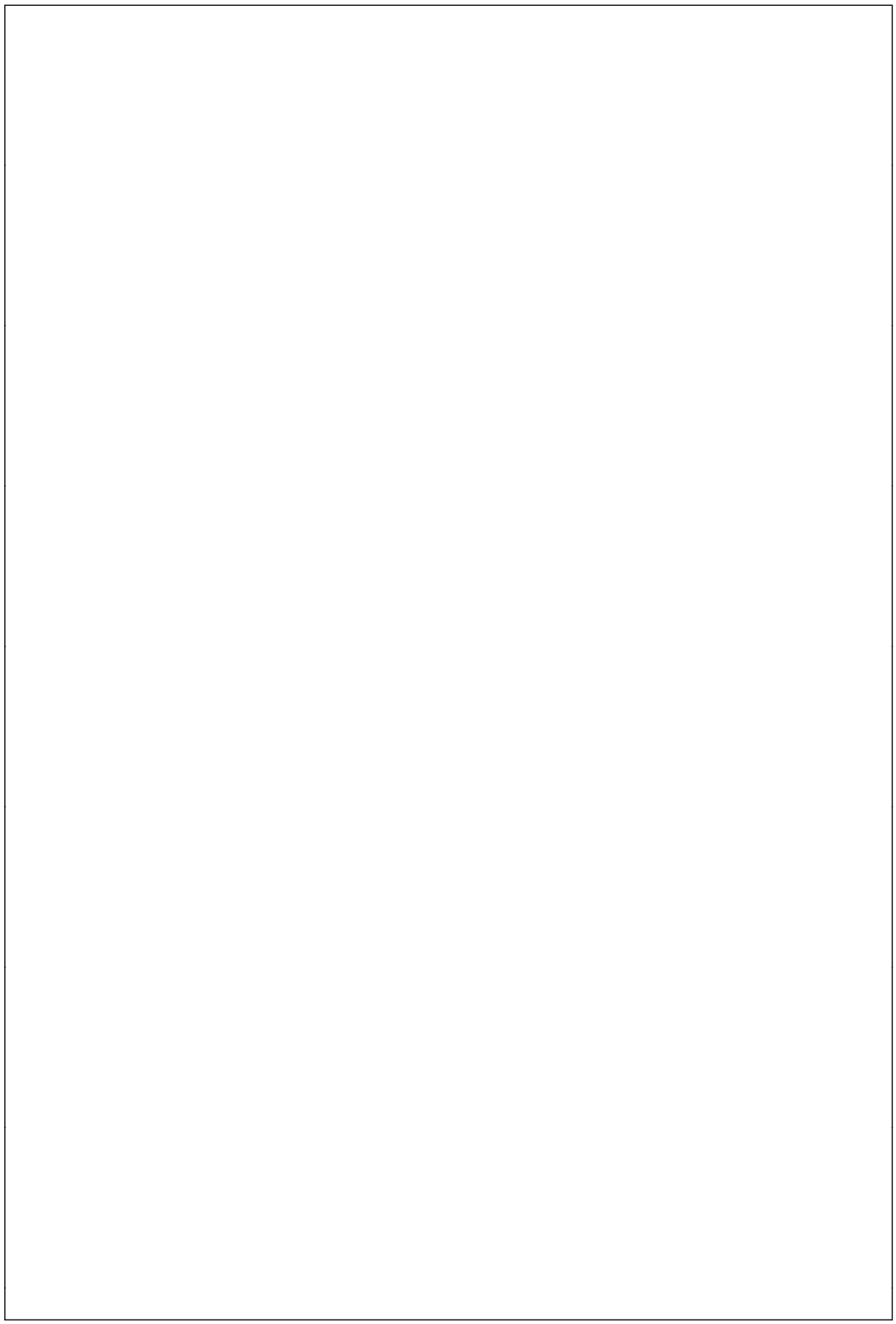
Order P/N: MOLE-DIAL-A-HLP

Information System Package Contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

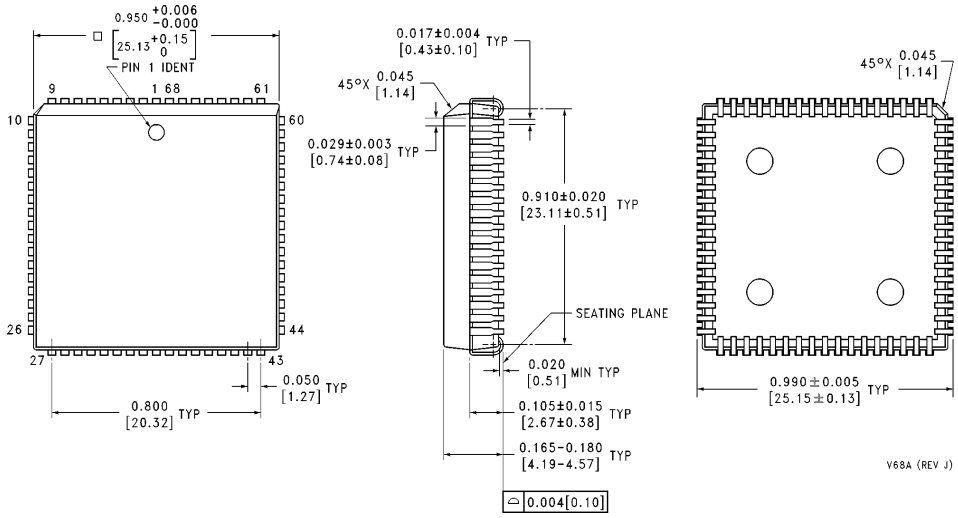
FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factory applications support. If a user is having difficulty in operating a development system, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 baud
Set-Up: Length: 8-Bit
Parity: None
Stop Bit: 1
Operation: 24 Hrs, 7 Days

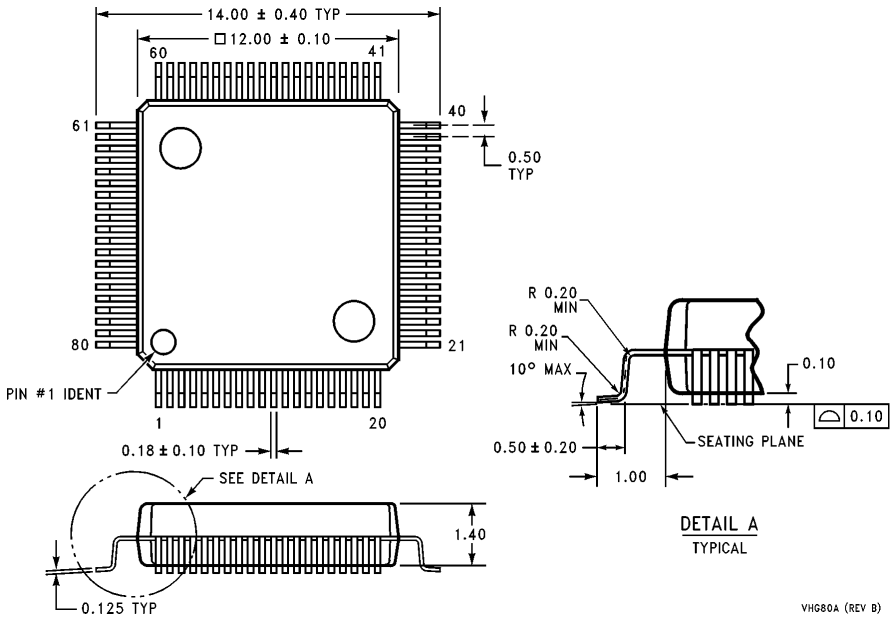


Physical Dimensions inches (millimeters)



Plastic Chip Carrier (V)
Order Number HPC46400EV or HPC36400EV
NS Package Number V68A

Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Flat Pack (PQFP)
Order Number
NS Package Number VHG80A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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